Provost’s Learning Innovations Grant for Faculty  
Request for Full Proposal  
2007-2008

Please hand-deliver your completed grant proposal (4 pages, plus attachments),  
the original plus 12 copies, to:  
Susan DeWoody, 1530 Wallace (5)  
by 4:30 p.m.  
No hand written proposals will be accepted.  
Notification of awards will be made by Friday, April 13, 2007. 

Project Title: LAB ON THE NETWORK

Applicant(s):

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<td>Dhireesha Kudithipudi</td>
<td>X5075</td>
<td>Computer Engineering</td>
<td>KGCOE</td>
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<td>P. R. Mukund</td>
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LAB ON THE NETWORK

Project Description

Complex systems, realized by integration of several components or subsystems, each of which can also be represented as a complex system, are increasingly employed in integrated circuits. The complexity of these systems leads to increasing cost of simulation and testing equipment. Some of these testing equipment are used by and large in most research/teaching labs in academia. However, the frequency of usage is limited by the turn-around time of the chips being fabricated. Usually fabrication of the chip from initial design to the final delivery time is around a year in most research labs. Even with a multitude of projects being performed in tandem, the effective time that the test equipment used in these labs is about 50%. During the intermediate idle phase, the testing equipment can be used by other research labs/students/faculty remotely. Other important factors that motivate the development of remote testing facility are the high equipment costs. A significant number of departments in various universities cannot afford the budgetary constraints imposed by this expensive equipment. One of the potential solutions to the problem is remote testing framework through internet. Remote testing (Lab on the Network) helps in distributed and shared learning experience for students/faculty/research labs by providing access to high cost equipment among different groups.

The goal of this project is to create an interactive “Lab Access Through Network” (LATN) for electrical and computer engineering students/research labs/faculty. The LATN testing framework can be accessed through the intranet/internet. The testing apparatus present at a remote location will be accessed through the LATN framework for testing a specific design (Design Under Test (DUT)). The framework can be visualized as three main components:
1) User End
2) Middleware
3) Remote Station

The user end will comprise of computer system(s) along with a probe station to mount the test chip. The middleware acts as a software/hardware interfacing unit to connect the probe station to the remote testing equipment. On the remote end, various testing units will be available, each connected through IEEE 488 (or General Purpose Interface Bus (GPIB)) bus. The GPIB bus connects and controls programmable instruments, and provides a standard interface for communication between instruments from different sources. Testing devices will be connected together on the bus in a daisy chained fashion.

The test chip will be mounted onto a probe station by the user. The mounted test fixture can be connected to different testing pins. The users can then establish connection to the remote testing equipment through a software interface. The test output obtained is available to the end user immediately. A dynamic database is maintained where results of test runs are stored. Users who test same chips can use the stored data for crosschecking the results from previous runs.

The software framework requires the user to create a testing script with the complete method which includes instrument selection and triggering as well as result interpretation and formatting. The user will have the flexibility to select specific instruments and invoke them. Once the testing script is submitted to the LATN system from an internet browser, the middleware software program opens a connection to a testing device running on the GPIB controller. The software program can also link to a plotting utility that returns test results in a graphical representation. Another part of the software converts user data to report format.
As a proof of concept, the testing resources available in both computer engineering and electrical engineering departments “RF Analog Mixed Signal” (RAM) lab will be used. The RAM lab will share the Agilent Technologies E8362A 45MHz - 20GHz PNA Series Network Analyzer ($30,000) and a Probe station ($10,000). The computer engineering department will share the Logic Analyzer ($12,000). Graduate student will aid in the development of the middleware for the LATN framework using Labview software. A web-based application and a database that ties to the middleware will also be developed using open-source software. The testing equipment will be interfaced to the middleware. Users will upload a test script through the web application. Middleware reads the test script and invokes the specified test equipment. Middleware also captures the test results and stores them in a database. The database that contains the test results can be accessed through the web interface.

**Targeted learners**

This project will help students in computer engineering and electrical engineering. The final product can be adopted in graduate level classes such as “Low Power VLSI Design”, “Mixed-Signal IC Design” and “Analog IC Design” where students from one department can use resources from the other department. Around 80~100 students take these courses each year. The final product can also be used as a case-study analysis for team projects. Also, all faculty and research labs in the college of engineering can use the end product for in-class demonstration and research.

**New Course or Current Course**

This project will be integrated with the current courses (“Low Power VLSI Design”, “Mixed-Signal IC Design”, “Analog IC Design”) that are offered in the electrical engineering and computer engineering.

**Anticipated Impact on Teaching and Learning**

**Teaching:**

- New opportunities for adopting the knowledge directly in to graduate courses “Low Power VLSI Design”, “Mixed signal IC Design”, and “Analog IC Design”.
- New strategies to enhance student learning by including the testing framework as part of the course curriculum.
- New design problems and case-study analysis for team-projects in the class.

**Learning:**

- New opportunities to learn about state of the art research as part of classroom lectures.
- Students can understand how a specific circuit design will impact the total performance of the system.

**Impact on Student Success**

RIT will be one of the few universities to implement such a system. Through this framework students will have access to a wide range of testing equipment which makes their learning experience exciting and challenging. Sharing distributed resources also provides the students with a collaborative learning experience and motivates them to actively participate in the classroom discussion. A similar approach is used within industry for their internal testing and thereby students are exposed to practices that are in place in the real-world. This will aid in preparing the students for co-op and job opportunities.
Report Findings

The effectiveness of the LATN framework will be assessed from the feedback of the students before and after the incorporation of the system in the relevant course work. Survey findings will be shared in the faculty meetings in both the departments. The findings will also be published in the engineering education journals such as IJEE, ASEE. The expertise in developing similar frameworks will be shared with interested faculty.

Rationale

a) The department of computer engineering currently does not have courses that use a remote testing experience. LATN framework can be incorporated into existing courses to share resources across the two departments. Since this is available over the internet, it is convenient to use the system for in-class demonstration.

Users can write test scripts off-line in any text editor and later load them onto the LATN system. Thereby the resources can be allocated to other users who are actively using the LATN system, enabling efficient sharing. Multiple users will be able to run testing queries on the “Design Under Test” by ordering the requests in a priority listing script. Equipment utilization is maximized, as user jobs are run sequentially from a wait queue.

b) Department of computer engineering and electrical engineering will be equipped with a dynamic LATN framework, which is currently unavailable. This framework can leverage the resources from one department to enhance the competency of the other department. Such domain will attract more students to actively participate in the courses which in-turn heightens their laboratory experience.

c) The developed framework will be accessible to all the faculty members in the college of engineering, who want to use the framework for research or teaching purpose.

d) Dr. P. R. Mukund is a Gleason Professor in the electrical engineering department. His research strengths are in RF and Analog I.C. Design. Dr. Mukund currently is the P.I. of three externally funded projects and has brought in over $2 million in external grants in the last four years. He has chaired many international conferences, was a distinguished lecturer of IEEE, and has published extensively in peer reviewed publications.

Dr. Dhireesha Kudithipudi is an assistant professor in the computer engineering department. Her research interests are “Fault-tolerant design for architectures in GHZ range”, “Low power design for nanoscale CMOS”, “Benchmarking for high performance processors”. She has published in journals and presented in several international conferences. She is currently in the technical program committee of IEEE workshop on “Unique Chips and Systems”.

Collaboration between these two faculty will provide mentoring for the success of junior faculty in attracting externally funded research. Further, it provides a model for successful teaming of faculty from different departments.

e) This dynamic testing framework will be conducive to use for courses in both electrical engineering and computer engineering department. Courses such as “Mixed Signal IC Design”, “Analog IC Design”, and “Low Power VLSI Design” can benefit from this framework. IC designs that are developed as part of the course curriculum can be tested using this framework.
Dynamic Remote Learning: - Although remote learning and web-based learning environments are popularly used pedagogical techniques in engineering curricula, the emphasis is on static repository sharing. In the proposed project, the users can use the testing tools on a network and the results are updated in the remote database which can be accessed by users, making it a dynamic repository learning experience. Users who perform similar tests do have facility to compare results from prior test runs.

Distributed Resource sharing: - The cost of test equipment can be prohibitively high for some academic and research labs. The remote testing approach can address this issue through resource sharing (of testing tools) and will provide a collaborative learning experience for users. The students will have access to resources otherwise not available in their respective departments.

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Support

The department of computer engineering is providing with a logic analyzer and the RAM lab from the electrical engineering department is supporting with a network analyzer and a probe station.