Evaluation of Single Phase Flow in Microchannels for High Heat Flux Chip Cooling—Thermohydraulic Performance Enhancement and Fabrication Technology

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The increased circuit density on today’s computer chips is reaching the heat dissipation limits for air-cooling technology. The direct liquid cooling of chips is being considered as a viable alternative. This paper reviews liquid cooling with internal flow channels in terms of technological options and challenges. The possibilities presented herein indicate a four- to ten-fold increase in heat flux over the air-cooled systems. The roadmap for single-phase cooling technology is presented to identify research opportunities in meeting the cooling demands of future IC chips. The use of three-dimensional microchannels that incorporate either microstructures in the channel or grooves in the channel surfaces may lead to significant enhancements in single-phase cooling. A simplified and well-established fabrication process is described to fabricate both classes of three-dimensional microchannels. Proof-of-concept microchannels are presented to demonstrate the efficacy of the fabrication process in fabricating complex microstructures within a microchannel.

A broad range of industries is driving the development of compact, advanced cooling technology. One of the most important of these applications is the removal of high heat fluxes in microelectronic circuitry. The continuing push toward more densely packed microchips will soon require greater thermal dissipation than can be provided by simple forced air cooling. Liquid cooling using fluid channels integrated onto the microchip is the next most attractive alternative [1]. This approach offers the advantages of a small footprint for packaging, reasonably low fluid flow rates, and potentially lower operating temperatures. However, issues such as reliability and functionality have to be addressed before microchannel cooling becomes widely adopted. It should also be recognized that unless a quantum leap in low-power device technology appears—analagous to the displacement of bipolar junction transistors (BJT) by...
complementary metal-oxide-semiconductor (CMOS) transistors—the inexorable increases in device density will produce heat fluxes beyond what even forced liquid cooling can provide.

Since the accommodation of large heat flux dissipation rates from a chip was demonstrated by Tuckerman and Pease [2] through the use of microchannel arrays, much of the research in the field has been focused on flow paths having constant cross-sections. Microchannel devices with simple rectangular, semi-circular, triangular, or trapezoidal shapes are readily fabricated and have been extensively studied in the literature (e.g., Nguyen and Wereley [3]). The performance improvement with small diameter channels was investigated by Kandlikar and Grande [4], who showed performance improvements achievable with microchannels (defined as channels with $10 \mu m < D_h \leq 200 \mu m$). As the industry enters the era of microchannel cooling, it makes sense to investigate all possible perturbations and enhancements that will improve the performance of microchannel-based coolers and extend their utility to the microelectronics industry for as long as possible.

More geometrically complex microchannels may offer attractive performance advantages, but they have not been extensively investigated. In this paper, we evaluate the cooling limits of single-phase liquid cooling in plain channels and explore the use of three-dimensional microchannel flow passages that incorporate a variety of microstructures into the channels for heat transfer enhancement. We refer to these as three-dimensional microchannels because their cross-sectional geometry varies along the flow length. Recently, a number of investigators have explored the use of three-dimensional microchannels. Complex serpentine flow channels for improved passive mixing have been built using the two-sided wet chemical etching of silicon wafers (Liu et al. [5]). The geometry of the device, however, makes it incompatible with integrated circuit cooling applications. Polymeric microchannels with corrugated walls have been analyzed and demonstrated for flow control and mixing by Stroock et al. [6, 7]. The materials of construction and the fabrication methods cannot be translated into the chip cooling arena. Thus, it does not appear that three-dimensional microchannels have been investigated for high flux heat transfer applications, possibly because of a limited understanding of their heat transfer and pressure drop characteristics and because of their increased fabrication complexity. In this paper, the requirements for high heat flux integrated circuit cooling are reviewed, the conventional engineering approaches are examined, and several three-dimensional device geometries that may offer important performance enhancements for microchannel-based high flux cooling systems are further explored from a fabrication standpoint.

**OVERVIEW OF CURRENT CHIP COOLING OPTIONS**

Heat removal from IC chips has been a major limiting factor in the development of microprocessors for computer systems. Although aggressive cooling technologies (such as compact heat exchanger passages or heat sinks with heat pipes) have been employed for specific high-end computing systems, the workhorse for the vast majority of computer applications continues to be air-cooling technology.

Air cooling integrated circuit chips has been extensively used because of the following attractive features: good compatibility with the microelectronic circuit environment, low auxiliary system support requirements, high reliability of the cooling system, low initial system cost, low operating and maintenance costs, and long developmental history and experience. However, there are a number of shortcomings associated with air cooling systems, such as low power dissipation potential, fan noise, and operational difficulties in dusty environments.

The main concern for air-cooling systems is their low heat removal potential. This arises from the low specific heat of air, which requires larger mass flow rates to achieve cooling. Moreover, the high specific volume of air leads to very large volumetric flow rates and their resulting high pumping costs and pressure drops creating fans that can deliver large volumetric flow rates at relatively large pressure heads without excessive noise levels poses a major design challenge in the air mover design. A good discussion on the fluid selection for cooling with internal flow channels is given by [8].

The low heat transfer coefficients associated with air-cooling systems necessitate the use of heat spreaders in an effort to increase the heat transfer surface area for convection. Figure 1 shows a schematic of an air-cooled system. Its equivalent thermal circuit is also shown. The
three main thermal resistances between the chip and the air are:

\[ \Theta_{\text{Cement}} \]: thermal resistance of the cement used to bond the chip to the heat spreader; also includes the contact resistances between the chip and the cement and the cement and the heat spreader.

\[ \Theta_{\text{Heat Spreader}} \]: thermal resistance of the heat spreader.

\[ \Theta_{\text{Convection}} \]: thermal resistance due to convection between the fins and the air.

Significant efforts have been directed toward reducing each of the three resistances. The heat spreader design evolved from conduction in a copper base to a thermosiphon loop transferring heat from the base to the hollow extended surfaces. The convective resistance has been reduced by increased air flow velocity, surface area, and heat transfer coefficient. The combination of thermosiphon loops and compact air flow passages (with their higher pressure drop penalties) have made the heat spreader and convective resistances quite low (e.g., 0.05°C·cm²/W for a commercial finned unit).

In spite of the considerable research directed toward lowering the thermal resistance of the cement, it still represents a major resistance in the thermal circuit. The use of specially formulated high conductivity cements, controlling their thickness to a very low value and providing very smooth surfaces, has resulted in a \( \Theta_{\text{Cement}} \) of as low as 0.1°C·cm²/W. With a heat flux density of 100 W/cm², this translates into a 10°C drop across the chip and the heat spreader. This value is quite large, considering that the total temperature differential available (LMTD for single-phase flow) may be only 40–50°C.

It becomes clear that increasing the allowable chip power dissipation rates will require considerable reductions in the thermal resistance between the chip and the heat spreader. The requirements of a thick base of high thermal conductivity material for the heat spreader and a good bond between silicon and the heat spreader make it difficult to lower \( \Theta_{\text{Cement}} \) any further.

Another major factor that limits further reduction in the thickness of the thermal cement is the difference in the thermal expansion coefficients for copper and the silicon substrate. Reducing the cement thickness causes much higher thermal stresses in the silicon substrate, leading to its mechanical failure. Direct cooling of the chips completely eliminates the contact resistance and associated thermal expansion problem. The incorporation of parallel, high aspect ratio microchannels further increases the convective heat transfer surface area and the heat transfer coefficient. These and other issues associated with direct liquid cooling are addressed, and the channel geometrical design is discussed to serve as a guideline in the design of the coolant passages.

**DIRECT COOLING WITH WATER—DESIGN CONSIDERATIONS**

Direct circulation of a fluid in channels fabricated on the chip eliminates altogether the thermal resistance associated with the cement used in mounting heat sinks. In this regard, the superior thermal properties (high specific heat, density, and thermal conductivity) of liquid water over refrigerants and air make it a desirable fluid for direct cooling. The incompatibility of water with electrical components can be overcome by using the back side of the chip for liquid flow passages. Although it is undesirable to subject the finished chips to microchannel fabrication from a manufacturing standpoint, improvements in the microchannel fabrication technology are expected to provide a very high yield to keep the costs under control. Nakayama [9] clearly brings out the superiority of direct water cooling, especially in conjunction with microchannels. The use of external heat sinks with liquid cooled microchannels has also been extensively studied in the literature (e.g., Missaggia et al. [10] and Bower et al. [11]).

Consider a chip that generates \( q \) watts and has its back surface area \( A_c \) available for heat dissipation. A simple analysis neglecting the conjugate effects in the substrate is performed to show the need for microchannel flow passages. For circulating water in a rectangular channel formed on the back surface, as shown in Figure 2, the minimum heat transfer coefficient required to meet the design goal is given by:

\[
h = \frac{q}{A_c \theta_{\text{LMTD}}} = \frac{q''}{\theta_{\text{LMTD}}}
\]

where \( q'' \) is the heat flux at the chip surface and \( \theta_{\text{LMTD}} \) is the log-mean temperature difference between the chip and the heat spreader.

**Figure 2** Top and cross-sectional views of the flow channel for water utilizing the back surface of the chip for cooling.
surface temperature, also assumed to be constant in this preliminary system level analysis, and the water inlet and outlet temperatures \( (T_{w,i} \text{ and } T_{w,o}, \text{ respectively}) \).

Figure 3 shows the variation of the heat transfer coefficient \( h \) needed to meet the cooling requirement as a function of heat flux for a chip surface temperature \( T_c = 85^\circ\text{C} \) and water inlet and outlet temperatures of \( T_{w,i} = 20^\circ\text{C} \) and \( T_{w,o} = 40^\circ\text{C} \), respectively. For a heat flux corresponding to 20 W/cm\(^2\) (∼50 W/in\(^2\)), a heat transfer coefficient of around 3,677 W/m\(^2\)-C is needed, whereas for a heat flux of 200 W/cm\(^2\) (∼500 W/in\(^2\)), \( h = 36,770 \text{ W/m}^2\text{-C} \) is needed.

Now consider the simple cooling system with water flowing over the chip surface in a rectangular channel, as shown in Figure 2. To achieve the desired heat transfer coefficients, it is imperative that a small hydraulic diameter channel be used. The flow in such small channels is expected to be laminar. For a nominal channel width of 25 mm (∼1 inch) and a channel length \( L \) of 25 mm, the variation of heat transfer coefficient with the gap height \( g \) is obtained by the following equations for a constant heat flux boundary condition. The actual dimensions are chosen for illustrative purposes only and have no effect on the result showing the need for microchannel flow passages. The hydraulic diameter of the rectangular channel is given by:

\[
D_h = \frac{4 \cdot gw}{2(g + w)} \quad (2)
\]

where \( g \) is the gap between the chip surface and the top cover and \( w \) is the width of the channel (assumed to be 25 mm). The Nusselt number for the constant heat flux boundary condition is dependent on the channel aspect ratio and is given by Kakac et al. [12]:

\[
Nu = 8.235(1 - 2.0421\alpha + 3.0853\alpha^2 - 2.4765\alpha^3 + 1.0578\alpha^4 - 0.1861\alpha^5) \quad (3)
\]

where \( \alpha \) is the channel aspect ratio, \( \alpha = g/w \). The resulting heat transfer coefficient, \( h = \frac{Nu \cdot k}{D_h} \), is plotted as a function of the gap \( g \) in Figure 4. The water properties are calculated at a mean temperature of 57.5°C. Although the actual heat transfer coefficient is higher due to the developing flow conditions along the length, the results presented in Figure 4 illustrate the relative magnitude of the heat transfer rates associated with plain channels.

It is seen from Figure 4 that a gap size on the order of 1 mm yields a heat transfer coefficient of 2370 W/m\(^2\)-C, which corresponds to a heat flux of only 22 W/cm\(^2\), as seen from Figure 3. Reducing the gap size to 100 \( \mu \text{m} \) yields a heat transfer coefficient of 24,600 W/m\(^2\)-C, which corresponds to a heat flux of about 175 W/cm\(^2\) in Figure 3.

Although providing rectangular cooling passages of 100 \( \mu \text{m} \) or smaller extends the chip power to over 100 W/cm\(^2\), the pressure drop for water flowing through the rectangular cooling channel becomes quite large. The water flow rate increases directly with the chip power for the fixed water inlet and outlet temperatures, and is given by:

\[
\dot{m} = \frac{q}{c_p(T_{w,o} - T_{w,i})} \quad (4)
\]

The frictional pressure drop of water flowing through the rectangular channel is given by the following equation:

\[
\Delta p = \frac{2fL\rho V^2}{D_h} \quad (5)
\]

where \( V \) is the mean flow velocity, \( L \) is the flow length, \( \rho \) is the fluid density, and \( f \) is the friction factor, which depends on the channel aspect ratio.

For laminar flow conditions, the product \( f \cdot \text{Re} \) is given by the following equation (Kakac et al. [12]):

\[
f \cdot \text{Re} = 24(1 - 1.3553\alpha + 1.9467\alpha^2 - 1.701\alpha^3 + 0.9564\alpha^4 - 0.2537\alpha^5) \quad (6)
\]
Figure 5 The variation of pressure drop with a gap height for water flow in a 25 mm-wide rectangular channel.

Figure 5 shows the frictional pressure drop for water flow plotted as a function of the chip power, calculated using Eqs. (4) and (5). It is seen from Figure 5 that the pressure drop increases dramatically below 0.1 to 0.2 mm gap sizes. For example, for 0.1 mm gap size, the pressure drop is close to 1 bar for \( q'' = 100 \text{ W/cm}^2 \).

The high pressure drop is not desirable. Besides the pumping power considerations, the silicon chip, which is generally 525–775 \( \mu \text{m} \) thick, may not be able to sustain the mechanical stresses.

**NEED FOR MICROCHANNELS AND ENHANCEMENT**

The cooling requirements of 100 W/cm\(^2\) and above cannot be easily met with either air cooling or, as discussed in the above section, with the simple water-cooling system shown in Figure 2. In order to meet this requirement, we need to increase the product of \( hA \), where \( h \) is the heat transfer coefficient and \( A \) is the heat transfer surface area. Since \( h \) is related to the channel hydraulic diameter, increasing the surface area \( A \) is another viable option. The heat transfer surface area \( A \) can be increased by incorporating microchannels on the chip surface, as shown in Figure 6.

The flow characteristics of water inside the microchannels are determined by the channel hydraulic diameter and cross-sectional area available for flow. From a heat transfer perspective, a smaller channel hydraulic diameter and larger channel surface area are favored. This leads to a large number of deep narrow channels, as shown in Figure 6. However, to accommodate the necessary mass flow rate through the microchannels, a large flow cross-sectional area is beneficial. A detailed analysis for such channels is investigated by a number of researchers, such as, Upadhye and Kandlikar [13].

As an example of potential area enhancement possibilities, consider the incorporation of simple pin fins in a square channel \( 300 \times 300 \mu \text{m} \) in cross-section. Placing pin fins of 30 \( \mu \text{m} \) diameter and 60 \( \mu \text{m} \) height at a pitch of 60 \( \mu \text{m} \) over the base would provide an area enhancement ratio of 2.57 over a flat-bottomed channel. Such enhancement structures are difficult and expensive to manufacture in macroscopic channels using conventional methods but can be easily manufactured in silicon microchannels by standard microfabrication techniques.

As seen from the above discussion, the heat transfer surface area and channel hydraulic diameter directly affect the heat transfer performance, while the hydraulic diameter and channel cross-sectional area affect the pressure drop. The desired feature is thus to have a large channel cross-sectional area in conjunction with a high heat transfer coefficient. These requirements can be met with the next generation of microchannels incorporating somewhat larger hydraulic diameters providing a larger cross-sectional area, and using heat transfer enhancement features.

Single-phase enhancement technology has been extensively investigated in the literature and is commonly employed in industry. Tao et al. [14] discuss different heat transfer mechanisms associated with different enhancement techniques in conventional sized channels. Bergles [15], in one of his recent summary articles on enhancement technology, proposes combinations of various enhancement strategies in the next generation of enhancement techniques. Steinke and Kandlikar [16] present a summary of conventional single-phase enhancement strategies for microchannel applications.

Various techniques have been utilized for single-phase heat transfer coefficient enhancements in laminar flows. After reviewing various enhancement approaches, the following techniques seem to hold promise in microchannel application:

- Increase in surface area through pin fins of circular, rectangular, or other streamlined cross-sections;
- Increase in surface area and heat transfer coefficient through interrupted and staggered strip-fin design, or any other advanced design similar to the compact heat exchanger surfaces;
- Increase in local heat transfer coefficient by breaking the boundary layer through periodic flow constrictions;
• Incorporation of grooves and ridges, at specified angles to the flow direction, to achieve heat transfer enhancement similar to microfin tubes;
• Incorporation of mixing features to improve the mixing between the bulk of the flow and the fluid flowing adjacent to the channel walls.

The thermohydraulic performance evaluation in terms of heat transfer and pressure drop characteristics of various enhancement techniques is essential before implementing them in practical devices. Such a study can be undertaken by conducting numerical simulation using CFD software, as well as through experimental evaluation. In addition, micro-PIV techniques are recommended to validate the flow characteristics from numerical code. Another major issue would be manufacturing considerations using silicon microfabrication technology, which is discussed further in the next section.

From a microfabrication standpoint, the enhancement strategies listed above can be grouped into two distinct classes of three-dimensional microchannel devices: those that require microstructures within the channel itself and those that require microstructures or grooves on the surfaces of microchannel walls. In the remainder of this work, a simplified fabrication process for building both classes of devices will be described. Proof-of-concept prototypes were constructed to confirm the utility of the process scheme.

**DEEP REACTIVE ION ETCHING TECHNOLOGY**

The need for deep, narrow flow channels requires high aspect ratio microfabrication technology. Reactive ion etching (RIE) techniques have served the semiconductor industry since the early 1970s. RIE is carried out in a capacitatively coupled parallel plate configuration and is simple, robust, and easy to maintain. Unfortunately, while RIE can be tuned to produce vertical structures, etch rates tend to be low, making the fabrication of deep channels an excessively time-consuming and expensive process. In the 1990s, a number of advances emerged in high aspect ratio etch technology. Of particular interest are the deep reactive ion etch (DRIE) processes, which combine high density plasma reactor designs with effective methods to suppress the erosion of the sidewalls. The most commercially prominent DRIE technique is the so-called Bosch process, which was invented by Larmer and Schilp [17] and is readily available from several equipment manufacturers. The microfabricated channels described in this work were etched in a standard DRIE tool. The novel multiple mask process developed and demonstrated here should be easily adapted to any standard tool.

**MICROSTRUCTURES WITHIN CHANNELS**

The fabrication of microstructures formed within the microchannels is discussed first. The features considered here all characteristically protrude from the “floors” of the channels.

The most straightforward method of producing structures in microchannels is to use the same patterned mask material that defines the edges of the microchannel itself. The microstructures that are fabricated in this manner will have the general appearance shown in Figure 7, where the height of the features is equal to the depth of the channel. The possible geometries are virtually limitless, constrained only by lithographic and processing considerations. A few representative structures such as fins, posts, and T-shaped fins are depicted in the figure. The inset shows a top view of the device, and also how the necessary etch mask would have to be lithographically patterned. In addition to modifying the heat transfer characteristics, the structures within the channels can serve other purposes such as filtering, flow control, and structural rigidity.

In the simple case of Figure 7, the height of the structures in the channels is the same as the depth of the microchannel. The tops of the features are coincident with the unetched substrate surface. In a more complicated, related configuration, the structures in the channel do not all have to possess the same height. An example is shown in Figure 8, where for simplicity only a set of fins is depicted.

It should be recognized that the geometrical freedom to design microstructures of the arbitrary shape described in Figure 7 applies equally to this case. Additionally, it is possible to have more than two different

**Figure 7** A microchannel with a variety of structures in the channel. The height of the structures is equal to the depth of the channel. The inset shows a top view.
heights to the structures in the microchannel. Indeed, the technique generalizes to an arbitrary number of distinct structure heights, and it is possible to assign any height to any structure.

**Fabrication Considerations**

The microstructures shown in Figure 7 do not require a fabrication sequence any more complex than that required for simple microchannels. Such structures can be realized by appropriately patterning the etch mask to include spatial information about both the features and the channel walls.

Microstructures whose heights differ from the channel depth, such as the short fins in Figure 8, require a more complex fabrication sequence. There are several possible processing approaches. The conventional method would be to use two cycles of lithographic patterning and etching, as illustrated in Figure 9. In this processing sequence, a first etch produces trenches of an intermediate depth. A second patterning step, shown in Figure 9(c), is necessary to define the shallow microstructures. This is the most problematic part of the process for several reasons. Since it is desirable to leave the first masking material in place, the choice of material for the second masking layer is subject to severe compatibility constraints. The deposition process and the patterning chemistries of the second mask layer cannot degrade the first mask. An even more daunting challenge is successfully photopatterning the second mask layer in the presence of severe topology. In realistic microchannel heat transfer devices, the second mask layer may need to be aligned and patterned at the bottom of a high aspect ratio channel several hundred microns in depth. This makes the fabrication of fine shallow structures extremely difficult.

A technique called one-step two-level etching (OSTLE) offers a simpler approach (see Grande et al. [18]). The use of this well-established process provides a relatively inexpensive method of producing complex microchannel structures. As shown in Figure 10, OSTLE requires two distinct lithography steps that are carried out sequentially before any significant topology is built up. The key to the technique is that in an ion-assisted process such as DRIE, the wafer experiences both a physical as well as a chemical component of attack. The physical etch component, caused by ion bombardment, produces a steady erosion of the etch mask. When fabricating simple features, such as those in Figure 7, the etch mask is intended to protect the underlying region of the substrate throughout the duration of the etching process. The erosion rate of the masking material, then, sets a minimum thickness for the mask to ensure that it is never completely removed. In the OSTLE technique, features with different heights can be produced by using two distinct masking layers: one that is impermeable to the etch and another that is erodible. The impermeable mask is thick enough to protect the underlying substrate for the entire etch process. The mask may be thinned by ion bombardment, but it never disappears altogether. The erodible mask, in contrast, is designed to ablate completely away at the point in the etch process where the etch depth equals the intended height of the shallow features. The

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**Figure 8**  A microchannel with finned structures of various heights. The inset shows a top view.

**Figure 9**  The conventional formation of shallow and deep features: (a) pattern mask to define deep features, (b) etch to an intermediate depth, (c) pattern mask to define shallow features, (d) etch to final depth, and (e) no masking layers.
The use of the OSTLE process: (a) erodible mask to define shallow features, (b) impermeable mask to define deep features, (c) etch to depth, and (d) removal of masking layers.

Figure 10 The use of the OSTLE process: (a) erodible mask to define shallow features, (b) impermeable mask to define deep features, (c) etch to depth, and (d) removal of masking layers.

Thermally grown silicon dioxide was used as the erodible mask. The etch rate ratio of silicon to silicon dioxide is a strong function of all the process parameters. Figure 11 illustrates the general behavior of the etch rate ratio with the reactive ion etch (RIE) power, which is applied to the sample platen, and the inductively coupled plasma (ICP) power, which produces the chamber plasma. Other process parameters, such as gas flow rates, pressure, loading conditions, and even the exact details of feature sizes will also affect the ratio. To illustrate the range of thicknesses of thermal oxide required to serve as an erodible mask, consider the data of Figure 11 at typical etch conditions of 12 watts RIE power and 600 watts of ICP power. At these settings, the etch rate ratio of silicon to silicon dioxide is approximately 350. This means that shallow features with a height of 50 \( \mu \text{m} \) would require an erodible mask of about 0.14 \( \mu \text{m} \) thickness. Such a thin film should present no topographical difficulties in the patterning of the impermeable mask.

In our experimental work, the silicon dioxide layer was grown using a standard wet oxide recipe to a thickness of 0.28 \( \mu \text{m} \) and then patterned using contact lithography and wet etching in buffered hydrofluoric acid. The impermeable mask was patterned using Shipley 812 photoresist spun to a thickness of 1.15 \( \mu \text{m} \). A pair of photomasks was designed with a variety of features including posts and fins and printed as a transparency on an imagesetter (Grande [19]). After the patterning of the impermeable mask, a DRIE process was carried out. The ICP power and RIE power were 600 W and 12 W, respectively. Other process conditions were 130 sccm SF\(_6\), 85 sccm C\(_4\)F\(_8\), a 12 second etch cycle, a 7 second passivation cycle, and a pressure control valve setting of 78. The measured depth of the microchannels was
A scanning electron micrograph of posts within a microchannel. Successive rows of posts are alternately tall and shallow. Tall posts are approximately 90 \( \mu \text{m} \) in height, equal to the depth of the microchannel. Shallow posts are approximately 60 \( \mu \text{m} \) in height. The shallow features had a height of 60 \( \mu \text{m} \). The observed etch rate ratio was 214. The disparity in etch rate ratio in this work versus the data of Figure 11 can be attributed to a smaller pressure control valve setting, loading effects, and feature size differences. This discrepancy demonstrates that careful process control is necessary to accurately hold target depths. Figure 12 shows one of the resultant microchannels.

The microchannel shown in Figure 12 is 500 \( \mu \text{m} \) wide and approximately 90 \( \mu \text{m} \) deep. The repeated microstructure pattern within the microchannel is a row of four posts inclined at 45\( ^\circ \) to the direction of flow. The posts have a diameter of about 80 \( \mu \text{m} \). It can be clearly seen that the rows alternate between tall posts with a height equal to the depth of the channel and shallow posts having a height of about 60 \( \mu \text{m} \).

It should be noted that the height of the shallow structures can be controlled over a very broad range. The thermal growth of silicon dioxide is an extremely well developed technology because of the material’s use as a gate dielectric in transistors. Current manufacturing processes can produce uniform thicknesses of thermal oxide down to a few nanometers (Sze [20]). At the lower range of the silicon-to-silicon dioxide etch selectivity shown in Figure 11, it should be possible to create shallow features with heights on the order of a micron. At the other extreme, a 1 \( \mu \text{m} \) thick erodible mask coupled with high etch selectivity processing conditions could produce shallow features of 500–600 \( \mu \text{m} \) height. Clearly, the shallow features can be tailored to range from dimensions comparable to the microchannels themselves down to dimensions that look like controlled surface roughness.

MICROSTRUCTURES WITHIN THE MICROCHANNEL WALLS

In this section, we examine the use of structures formed in the sidewalls as well as the floor of the microchannels. The structures form grooves in the surfaces of the channels. Figure 13 illustrates several types of structures, including grooves perpendicular to the direction of flow, grooves inclined at 45\( ^\circ \) to the direction...
A geometrical layout of mask materials for (a) microstructures within microchannels, and (b) microstructures formed within the sidewalls of a microchannel.

Figure 14

Figure 15 A scanning electron micrograph of a microchannel with chevron-shaped grooves etched into the floor of the channel. The grooves extend vertically upwards at the sidewalls. The microchannels are approximately 500 µm wide and 30 µm deep. The grooves are etched approximately 60 µm into the “floor” of the channel.

DISCUSSION

Given the high level of understanding of single-phase heat transfer phenomena in plain and enhanced geometries and the current status of microfabrication technology, a case can be made to seriously consider implementing enhancement features in microchannel flow passages for high heat flux chip cooling. However, there are a number of issues that must be addressed before widespread application of these techniques becomes a reality.

Pressure Drop Considerations

The improvement in the thermal performance of enhanced 3-D structures is accompanied by an increase in pressure drop. A careful analysis needs to be performed to evaluate the suitability of these structures for specific applications with regard to the maximum allowable system pressure as well as the size and cost considerations for the pumping system. Although the pressure drops per unit length are higher, it is imperative that the microchannel heat exchangers will employ single-pass design with shorter passage lengths. The pumping power needs to be evaluated under a new paradigm that addresses the benefits of single-phase microchannel cooling as opposed to the more complex systems incorporating phase change and/or spray or jet cooling techniques. This paradigm shift is expected to be similar to that experienced in automotive compact heat exchanger applications, where higher pressure drops are accepted due to associated size and weight benefits over heat exchangers employing conventional size channels.
Further, it is expected that incorporating smaller channel lengths will permit the heat exchanger design within the specified design envelope.

**Experimental Verification of Design**

The development of specific 3-D structures poses another major challenge. Working from a design concept, preliminary CFD analysis would provide guidance in this area. However, experimental verification is essential to address issues such as flow maldistribution, entrance region effects, variability introduced in the channel size and shape by the manufacturing process, substrate heat conduction, localized hot spots, fin efficiency, and localized variation of heat transfer coefficients. It should be emphasized here that heat transfer and pressure drop experiments pose special measurement challenges, as highlighted by Kandlikar [21].

**Fouling Considerations**

Although clean fluids will be employed, fouling due to the interaction of various piping and pump materials with silicon microstructures has not been investigated. This research is expected to set standards for cleanliness and the additives required for reliable long-term performance of 3-D enhanced single-phase cooling systems.

**Manufacturing Technology and Costs**

Although incorporating 3-D silicon enhancement structures is not expected to add significant costs to the microfabrication process itself, the major cost consideration will be overall yield. It seems preferable to build the microchannel cooling passages after the microelectronic circuitry is completed, rather than at the beginning of the process. At this stage, wafers in process represent high value, and the yield through the microchannel construction phase becomes critical. Manufacturing research will be required to demonstrate that issues such as wafer handling, increased wafer fragility, and backside processing do not lead to unacceptable yield losses.

**Comparison with Flow Boiling Systems**

The single-phase cooling option is preferable to the two-phase (boiling) option because of increased complexities associated with the boiling systems. Further, the saturation temperature becomes an issue with water, and one is forced to employ subatmospheric pressures for IC chip cooling. Additional issues such as dissolved gases, condensation equipment, nucleation site deactivation through fouling and hysteresis, need to be addressed. Although the two-phase systems are inherently capable of removing high heat fluxes through the latent heat transport, enhanced 3-D structures may be effective alternatives for intermediate heat fluxes, tentatively in the 100–300 W/cm² range.

**CONCLUSIONS**

Microchannel heat transfer applications have become more demanding in terms of performance and system integrability since the early 1980s. In this paper, the use of engineered structures within microchannels has been explored. The thermohydraulic benefits have been examined and realistic methods of fabrication have been described. Fabrication methodologies for two specific classes of devices, microchannels containing structures within the channel and those with grooves etched into the channel walls, have been proposed. Both types of devices have been successfully built and presented.

**NOMENCLATURE**

- \(A\) surface area, m²
- \(c_p\) specific heat, J/Kg K
- \(D\) diameter, m
- \(f\) friction factor, dimensionless
- \(g\) gap height, m
- \(h\) heat transfer coefficient, W/m² K
- \(k\) thermal conductivity, W/m K
- \(L\) length, m
- \(m\) mass flow rate, kg/s
- \(n\) number of channels, dimensionless
- \(Nu\) Nusselt number, dimensionless
- \(q\) power generation or heat removal rate, W
- \(q''\) heat flux, W/m²
- \(Q\) volume flow rate, m³/s
- \(Re\) Reynolds number, dimensionless
- \(t\) thickness, m
- \(T\) temperature, K
- \(V\) mean flow velocity, m/s
- \(w\) channel width, m

**Greek Symbols**

- \(α\) channel aspect ratio, g/w dimensionless
- \(Θ\) thermal resistance, K/W
- \(θ\) temperature difference, K
- \(μ\) dynamic viscosity, kg/m s
- \(ρ\) density of fluid, kg/m³
- \(Δp\) pressure drop, Pa
Subscripts and Superscripts

$c$  chip
$w,i$  water inlet
$w,o$  water outlet
$LMTD$  log mean temperature difference

REFERENCES


Satish Kandlikar has been a professor in the Mechanical Engineering Department at RIT for the last twenty-two years. He received his Ph.D. from the Indian Institute of Technology in Bombay in 1975 and has been a faculty member there before coming to RIT in 1980. His research is mainly focused on flow boiling. After investigating the flow boiling phenomenon from an empirical standpoint, which resulted in widely accepted correlations for different geometries, he started to look at the problem from a fundamental perspective. Using high-speed photography techniques, he demonstrated that small bubbles are released at a high frequency under flow conditions. His current work involves stabilizing flow boiling in microchannels, interface mechanics during rapid evaporation, and advanced chip cooling with single-phase liquid flow. He has published over 100 journal and conference papers. He is the Heat in History Editor of Heat Transfer Engineering and a fellow member of ASME, and he has been the organizer of the two international conferences on Microchannels and Minichannels sponsored by ASME. Visit www.rit.edu/~taleme for further information and publications.

William J. Grande has worked in the field of microfabrication for more than two decades. His research has centered on the fabrication tools, processes, and devices used in the areas of III-V lasers, optoelectronics, Microsystems, and MEMS. He holds undergraduate degrees in Electrical and Chemical Engineering and an M.S. and Ph.D. in Applied and Engineering Physics. He expects to complete the M.B.A. in 2004. In 1999, after ten years of industrial research experience at the IIT Research Institute and Kodak Research Labs, he joined the Microelectronic Engineering faculty at the Rochester Institute of Technology, where he expanded the curriculum and research efforts in Microsystems fabrication, particularly in the area of direct thick film writing. In 2004, Dr. Grande joined Ohmcraft, Inc. in Honeoye, New York, as Director of Research and Business Development. Dr. Grande holds sixteen patents and has several more pending. His research interests include novel microfabrication technologies, microfluidics, rapid prototyping, and nanotechnology. In 2000, Dr. Grande founded Tiger Microsystems, Inc., which specializes in the commercialization of microsystem-based products.