
Objective	To obtain a research position in the field nanotechnology to utilize my experience in microelectronic and microsystems engineering.
Education	<ul style="list-style-type: none">▪ Ph.D., Rochester Institute of Technology<ul style="list-style-type: none">▪ Major: Microsystems Engineering (current- expected graduation Q1 2013)▪ Research: Nanolithography▪ Masters of Science, Rochester Institute of Technology<ul style="list-style-type: none">▪ Major: Microelectronic Engineering, November 2008, GPA 4.0▪ Thesis: Development of a Plasma-Deposited Low Temperature Gate Dielectric▪ Bachelor of Science, Rochester Institute of Technology<ul style="list-style-type: none">▪ Major: Microelectronic Engineering, November 2005, GPA 3.575
Experience	<p>8/08-3/2010 Mentor Graphics Corp., imec, Leuven Belgium RET Technical Marketing Engineer</p> <ul style="list-style-type: none">• Double Patterning OPC development• DP design methodologies for the 22nm and 32nm nodes• EUV OPC & OPC model development• SEM contour calibration of OPC models• Inverse lithography for assist feature placement <p>8/05-8/08 Corning Incorporated, Rochester Institute of Technology, Rochester, NY Thin Film Transistor Process Engineer</p> <ul style="list-style-type: none">• Process Engineer for PVD, CVD, lithography, and several other processes• SiOG/ Low Temperature CMOS Process Team leader• Implemented process changes, significantly improving device yield and performance. <p>6/08-8/08 Kyung-Hee University ADRC, Seoul Korea Thin Film Transistor Gate oxide Engineer</p> <ul style="list-style-type: none">• Gate oxide engineering for TFT applications.• C-V and I-V testing of various gate dielectrics.• Advising of process integration projects in ADRC's process <p>3/05-12/05 BetaBatt, Rochester Institute of Technology, Rochester, NY Beta Voltaic Device Researcher</p> <ul style="list-style-type: none">• Designed/ Implemented second generation process• Characterized the porous silicon formation process• Implemented a RTA process for ultra shallow junctions• Silvaco SUPREME and Atlas simulations of photovoltaic devices <p>4/04-8/04 IT Collaboratory, Rochester Institute of Technology, Rochester, NY Process Development Intern</p> <ul style="list-style-type: none">• Low Stress PECVD TEOS & Nitride for MEMS applications• Isotropic Oxide/Nitride RIE <p>MEMS Research</p> <ul style="list-style-type: none">• Smart Microfluidic Systems on Dielectrophoresis and Electrowetting, involved in the implantation stage of MEMS device. Worked with other researches to develop further generations of devices• Robustness and Reliability for Micro-Actuators and Micro-Machinery, involved in second generation devices, helped implement future changes <p>6/03-12/03 Eastman Kodak Image Sensor Solutions, Rochester, NY LPCVD Process Engineer & Yield Engineer Intern</p> <ul style="list-style-type: none">• Changed polysilicon quartz ware from v-slot to y-slot, reducing particulate count- decreasing down-time• Change of polysilicon CVD hardware to improve film quality and optimizing the process with a DOE• Sustaining engineering for both atmospheric and LPCVD furnaces.• Reduced heavy metal contamination in the processing line, increasing yield by a reduction in dark current <p>Proficient problem solving skills, tcl, csh, perl, Calibre, Silvaco SUPREME, Atlas, JMP IN, MATLAB, and PROLITH. Hands on experience in clean room environment with a variety of equipment.</p>
Skills	
Accomplishments / Activities	Dpt. of Education GAANN PhD Fellowship, President of RIT SPIE Chapter, RIT MS Scholarship, BeTheMatch.org, Genesee River Cleanup, Victory Alliance, Presidential Service Merit Award, Honor Society, IEEE, ASM, SID, OSA, MESA, Oven Door Running Club, Rochester Bicycling Club, RAGBRAI

Public Publication List:

- G. Fenger, 2009. "Thin Film Transistor Having a Common Channel and Selectable Doping Configuration", US Patent Application 20090294853, filed Dec 2009, Patent Pending
- G. Fenger, B. W. Smith "Image-based EUVL Aberration Metrology" EIPBN June 2011
- G. Fenger, G. Lorusso, E. Hendrickx, A. Niroomand "Design Correction in Extreme Ultraviolet Lithography" J. Micro/Nanolith. MEMS MOEMS vol. 9, No. 4, Oct-Dec 2010
- D. Hibino, H. Shindo, Y. Abe, Y. Hojyo, G. Fenger, T. Do, I. Kusnadi, J. Sturtevant, P. De Bisschop, J. de Kerkhove "High-accuracy OPC-modeling by advanced CD-SEM based contours in the next-generation lithography" Proc. of SPIE Vol. 7638, 76381X, Feb 2010
- G. Lorusso, E. Hendrickx, G. Fenger, A. Niroomand "Full chip correction of EUV design" SPIE Vol. 7636, 763615 Feb. 2010
- G. Lorusso, F. Van Roey, E. Hendrickx, G. Fenger, M. Lam, C. Zuniga, M. Habib, H. Diab, J. Word, "Flare in extreme ultraviolet lithography: metrology, out-of-band radiation, fractal point-spread function, and flare map calibration" J. Micro/Nanolith. MEMS MOEMS vol 8(4), 041505 Oct-Dec 2009
- H. Shindo, A. Sugiyama, H. Komuro, Y. Hojyo, R. Matsuoka, J. Sturtevant, T. Do, I. Kusnadi, G. Fenger, P. De Bisschop, J. Van de Kerkhove, "High-precision contouring from SEM image in 32-nm lithography and beyond" Proc. of SPIE Vol. 7275, 72751F Feb. 2009
- K. Sakjiri, A. Trichtkov, Y. Granik, E. Hendrickx, G. Vandenberghe, M. Kempell, G. Fenger, K. Boehm, T. Scheruebl, "Application of Pixel-based Mask Optimization Technique for High Transmission Attenuated PSM" Proc. of SPIE Vol. 7275, 72750X, Feb. 2009
- R. Manley, G. Fenger, P. Meller, K. Hirschman, C. Kosik Williams, D. Dawson-Elli, J. G. Couillard, J. Cites, "Development of Integrated Electronics on Silicon-on-Glass (SiOG) Substrate" ECS Trans. Vol 16 (9) pp371 2008
- R. Manley, G. Fenger, P. Meller, K. Hirschman, C. Kosik Williams, D. Dawson-Elli, J. G. Couillard, J. Cites, "Development of Integrated Electronics on Silicon-on-Glass (SiOG) Substrate" Meet. Abstr. ECS 802 pp2328 2008
- D. Dawson-Elli, C. Kosik Williams, J. G. Couillard, J. Cites, R. Manley, G. Fenger, K. Hirschman, "Demonstration of High Performance TFTs on Silicon-on-Glass (SiOG) Substrate" ECS Trans. Vol 8 (1) pp223 2007
- D. Dawson-Elli, R. Manley, G. Fenger, K. Hirschman, J. G. Couillard, C. Kosik Williams, "Demonstration of High Performance Low Temperature Crystalline Silicon (LTCS) Thin-Film Transistors" Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors ECI, July 2007
- R. Manley, G. Fenger, K. Hirschman, J. G. Couillard, C. Kosik Williams, D. Dawson-Elli, J. Cites, "Demonstration of High Performance TFTs on Silicon-on-Glass (SiOG) Substrate" SID Symposium Digest of Technical Papers, Vol 38 Issue 1 pp 287-289, May 2007
- E. Woodard, R. Manley, G. Fenger, R. Saxer, K. Hirschman, D. Dawson-Elli, J. G. Couillard, "Low Temperature Dopant Activation for Integrated Electronics Applications" UGIM 25-28 pp161-168, June 2006

Private Publication list

- V. Wiaux, S. Verhaegen, G. Fenger, P. Wong, "Density Limits in Logic Metal1 using Double Patterning" 6th International Symposium on Immersion Lithography Extensions, Oct 2009
- G. Fenger, P. LaCour, A. Trichtkov, S. Komirenko, V. Wiaux, "Wafer and Simulation Study Comparing 5 LELE Decomposition Algorithms for Both Compliant and Non-Compliant Layouts" 6th International Symposium on Immersion Lithography Extensions, Oct 2009
- G. Lorusso, G. Fenger, A. Niroomand, E. Hendrickx, "IMEC TM08 Modeling and Validation" IMEC Advanced Litho PTW, Oct 2009
- V. Wiaux, P. Wong, D. Vangoidsenhoven, S. Verhaegen, J. Bekaert, T. Matsuda, Y. Nomura, A. Lin, G. Fenger, W. Gao, "SP2 Double Patterning summary and outlook" IMEC Advanced Litho PTW, Oct 2009
- T. Matsuda, V. Wiaux, Y. Nomura, G. Fenger, "Experimental density limitation for 32hp 2D metal interconnect using DP" IMEC Advanced Litho PTW, Oct 2009
- G. Lorusso, E. Hendrickx, J. Jiang, D. Lieberman, G. Fenger, M. Lam, S. Jang, L. Zavyalova "Model calibration and validation for EUV design correction" IMEC Advanced Litho PTW, Oct 2009
- G. Lorusso, G. Fenger, F. Van Roey, E. Hendrickx, "Accurate flare map generation for OPC modeling" IMEC Advanced Litho PTW, April 2009
- V. Wiaux, P. Wong, M. Maenhoudt, A. Miller, D. Vangoidsenhoven, V. Truffert, G. Murdoch, T. Matsuda, S. Irie, Y. Nomura, T. Sasaki, A. Lin, G. Fenger, W. Gao, K. Iwase, S. Postnikov, A. Niroomand, M. Dusa, S. Verhaegen, "SP2 - Double Patterning summary and outlook" IMEC Advanced Litho PTW, April 2009
- Lin, V. Wiaux, G. Fenger, "L113 2-masks FLASH using SDDP : simulation results" IMEC Advanced Litho PTW, April 2009
- T. Matsuda, V. Wiaux, Y. Nomura, G. Fenger, S. Verhaegen, T. Sasaki, "Improved resolution of split DP for LOGIC and DRAM" IMEC Advanced Litho PTW, April 2009
- T. Matsuda, V. Wiaux, S. Postnikov, G. Fenger, S. Verhaegen, "DP design split for 32nm hp Logic and DRAM Metal1" IMEC Advanced Litho PTW, October 2008