



Analysis of the Biasing Conditions and Latching Operation for Si/SiGe Resonant Interband Tunnel Diode Based Tunneling SRAM

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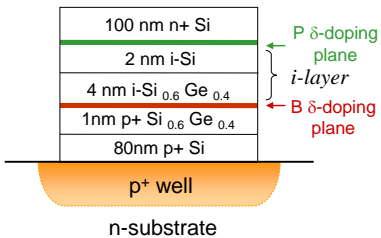
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Abstract

Two Si/SiGe resonant interband tunnel diodes (RITD) grown on top of p+ implanted wells with PVCR of 2.25 and peak current density of 2.15 kA/cm² were used to build a tunneling static random access memory (T-SRAM). A detailed analysis of the biasing conditions and latching operation to write and read the logic states was performed. A noise margin of 552 mV between logic high and low was obtained while using a relatively low power supply of 1 V.

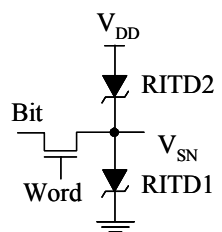
Si/SiGe Resonant Interband Tunnel Diode (RITD)



- Hybrid between Esaki diode and RTD.
- Fabricated Using Low Temperature Molecular Beam Epitaxy (LT-MBE).
- Utilize δ -plane.
- Intrinsic layer (i-layer) thickness determines current density.

Rommel, APL, 1998; Jin, TED, 2003

Tunnel Diode Based SRAM

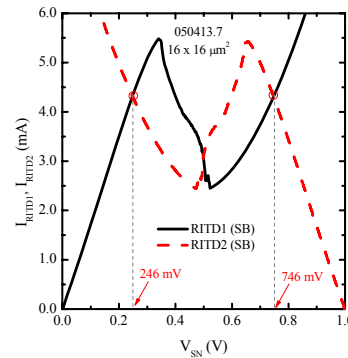


- First proposed by Goto et al. (*IRE TEC*, 1960) and the concept was refined by Van der Wagt (*Proc of IEEE*, 1999).
- It consists of two tunnel diodes in series with a FET connected into the middle node to modulate the current into the sense node (SN).
- RITD1 acts as the drive, and RITD2 acts as the load.

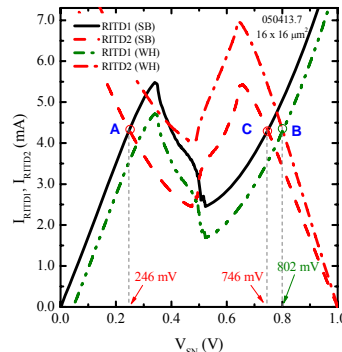
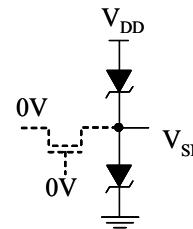


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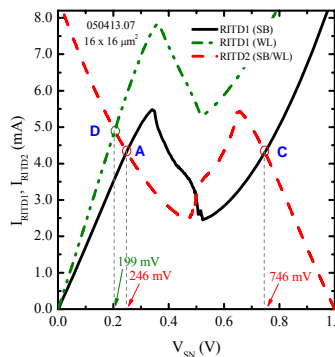
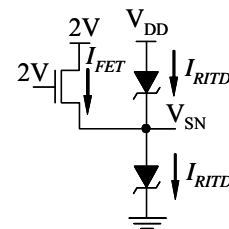
Latching Operations



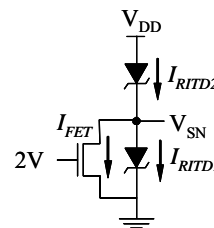
Stand-by



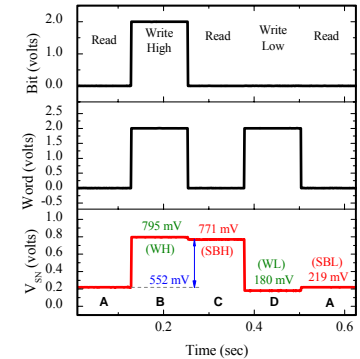
Write High



Write Low



Time Diagram



- Stand-by load provides the two possible latching points, **A** and **C**.
- During the write to logic high, latching point moves from **A** to **B** to **C**.
- During the write to logic low, latching point moves from **C** to **D** to **A**.

Performance Comparison with Other RITD-Based SRAM Cells

TSRAM A	TSRAM B	TSRAM C	TSRAM D	TSRAM E
Dynamic R-Load	Quasi-static R-Load	Dynamic FET-Load	Quasi-static FET-Load	Static RITD-Load
2 Components (1R+1TD)	3 Components (1R+1FET+1TD)	2 Components (1FET+1TD)	3 Components (2FET+1TD)	3 Components (1FET+2TD)
$\Delta V \sim 392$ mV	$\Delta V \sim 391$ mV	$\Delta V \sim 350$ mV	$\Delta V \sim 313$ mV	$\Delta V \sim 552$ mV
$V_{DD} = 1.2$ V	$V_{DD} = 1.2$ V	$V_{DD} = 2.0$ V	$V_{DD} = 2.0$ V	$V_{DD} = 1.0$ V
$P_{SB} = 4.96$ mW	$P_{SB} = 4.84$ mW	$P_{SB} = 9.77$ mW	$P_{SB} = 9.75$ mW	$P_{SB} = 4.34$ mW

Conclusion

Load line analysis is performed to understand the latching mechanism of Si/SiGe RITD based T-SRAM during the write and read cycles. This demonstration will lead to realization of fully-integrated Si/SiGe RITD/NMOS Tunneling SRAM. Ultra-low power tunneling SRAM can be achieved by utilizing low current density RITD.