Student Paper

High Temperature Characterization of Si/SiGe Resonant Interband Tunnel Diodes

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Co-integration of Si-based tunnel diodes and CMOS circuits has been proposed for several years as a means to lower power consumption, reduce operating voltage and shrink device count. Recently, the successful integration of Si/SiGe resonant interband tunnel diodes [1,2] with CMOS [3] was demonstrated with room temperature operation. However, integrated circuits realistically operate significantly above room temperature, usually around 373K. Therefore, SPICE models used by circuit designers must account for device performance variations due to temperature changes ranging from 300K to 473K. For circuit applications, the key tunnel diode parameters are the peak and valley current densities (J_p and J_v, respectively) as well as the peak-to-valley current ratio (PVCR). Previous high temperature studies on Si-based Esaki diodes [4-6] and Si/SiGe resonant interband tunnel diodes (RITD) [7] showed some dissimilar trends for PVCR. This study examines the high temperature operation of Si/SiGe RITD more closely up to 473K.

Figure 1 illustrates the schematic diagram of the various RITD structures investigated in this study. The intrinsic layer between the δ-doped planes consists of X nm of undoped Si and Y nm of undoped SiGe. Three different structures with 1nm/3nm, 2nm/4nm, and 4nm/4 nm of X/Y i-layer thicknesses, named TD-A, TD-B, and TD-C, respectively were fabricated using low temperature molecular beam epitaxy. The current-voltage characteristics of these devices were measured using a Keithley 4200 Semiconductor Parameter Analyzer. The temperature of the heat chuck was controlled via an ΩE Omega CSC32-J bench top controller. A thermocouple was mounted in direct contact with the wafer for all measurements. Initial measurements were taken at room temperature, with subsequent readings in 10K increments from 300K to 473K. Several measurements were also taken while the wafer was cooling down. Those results were consistent with the initial heat up measurements. The I-V characteristics were not found to vary significantly over a two hour time period for any particular temperature.

Figure 2 shows the I-V characteristics for device TD-C. The general shape of the curve remains the same over the entire temperature range. Figure 3 overlays valley currents normalized with respect to the room temperature valley current for TD-C as well as data from other published studies [5-7]. It should be noted that the normalized J_v data for TD-A and TD-B directly overlays TD-C and Jin's data [7]. Si/SiGe RITD valley current shows a weak temperature dependent signature. In contrast Esaki diodes formed by proximity annealing [5,6] exhibit a stronger temperature sensitivity. As illustrated in Fig. 4, the PVCR of TD-A, TD-B, and TD-C decreases as temperature increases. Device TD-A has a PVCR of 1.99 at 373 K. However, devices TD-B and TD-C resulted in PVCRs of 2.58 and 2.91 at 373 K, respectively.

Overall, there was no significant effect on the device characteristics from heating the Si/SiGe RITDs. The PVCRs observed at 373 K were found to be sufficient for digital circuit/memory circuit operation. These results conclusively demonstrate that high temperature operation will not be a limiting factor in CMOS/RITD circuitry.

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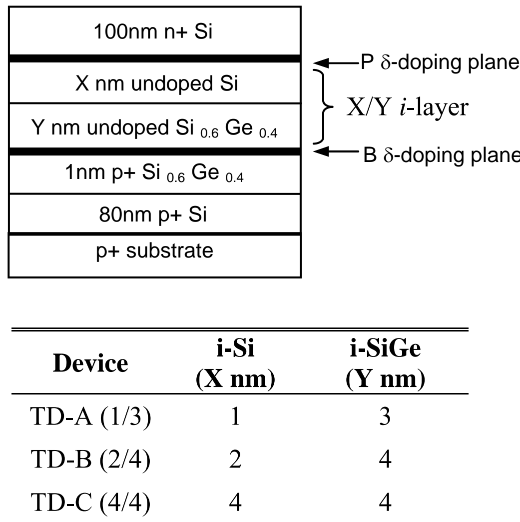

Device	i-Si (X nm)	i-SiGe (Y nm)
TD-A (1/3)	1	3
TD-B (2/4)	2	4
TD-C (4/4)	4	4

Fig. 1 Schematic diagram of Si/SiGe RITD with various X/Y i-layer thicknesses.

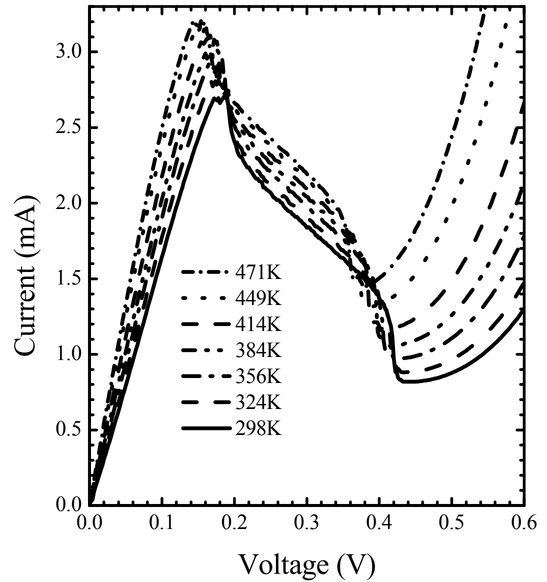

Fig. 2 I-V Characteristics of TD-C (4/4) at temperature ranging from 298K to 471K.

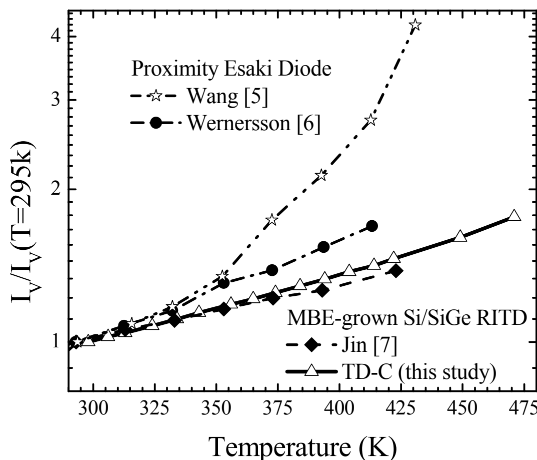

Fig. 3 J_V normalized by J_V at room temperature vs. temperature. TD-A and TD-B (not shown) overlap TD-C. The data is plotted against published results in refs. [5-7].

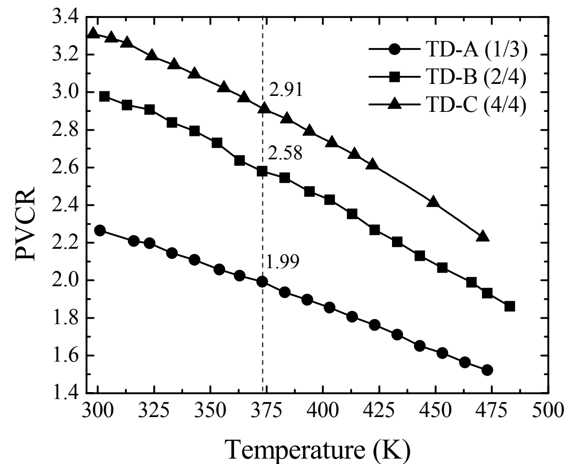

Fig. 4 PVCR as a function of applied temperature. TD-C exhibits a PVCR of 2.91 at 273K.