

QUANTUM AND SPIN TUNNEL DEVICES FOR MEMORY APPLICATIONS

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ABSTRACT

The increasing trend towards portable digital electronics and wireless communication devices has driven the advancement of several memory technologies in the last couple of decades. The standards of performance are becoming more stringent, posing several challenges from device design, circuit architecture, and manufacturing capability. The current commercially available memory devices, such as SRAM, DRAM, and Flash, offer enhanced performance in one aspect while sacrificing on other areas.

Memory technologies that utilize quantum tunneling based devices, such as tunneling diodes have been sought as a viable solution. The tunneling property allows for fast switching. The low operating voltage results in low standby power. Recent breakthroughs by the authors in monolithic integration of SiGe resonant interband tunnel diodes (RITDs) with CMOS devices offer novel architectures for memory applications. The latest developments demonstrated a refresh-free Si-based tunneling static random access memory (TSRAM), exhibiting an enhanced signal to noise ratio. In addition, its basic cell can be expanded into a multi-level memory by utilizing several tunnel diodes connected in series. This would substantially increase memory density.

Magnetic Random Access Memory (MRAM) uses electron spin to store data. MRAM has been called the “holy grail” of memory because it has the potential to combine the speed of SRAM, the density of DRAM, and the non-volatility of flash memory. It relies on spin-based tunneling devices, such as magnetic tunneling junctions (MTJs).

To further extend the versatility of tunnel diodes in a memory cell, a new initiative is being carried out to integrate Si-based RITDs with MTJs. This approach will add a non-volatility attribute, a valuable characteristic to overall memory architecture. It has been shown through physical models and simulations that a series combination of an MTJ and a tunneling diode increases the tunneling magnetoresistance ratio (TMR) significantly. A multi-valued magnetic RAM can also be achieved by employing ferromagnetic layers of various coercivities to form a double barrier MTJ. Four distinct states can be achieved through different combinations of magnetization directions of each free layer. To read the states, the non-linear characteristic of the tunneling diode would be utilized.

The introduction of quantum and spin tunneling devices opens up a new class of novel memory architectures. Most ideal characteristics of a memory system could be drastically improved.

INTRODUCTION

The confluence of the semiconductor industry and the magnetic recording industry has recently been triggered by the application Giant Magnetoresistive (GMR) structures into semiconductor beginning a new age of spintronics. Semiconductor-based spintronics could combine logic, storage and communications on a single chip. Microelectronic devices that function by using the spin of the electron are a nascent multibillion dollar industry – and may lead to quantum microchip. More sophisticated storage technologies based on spintronics are already at an advanced stage; with MRAM ready for market.

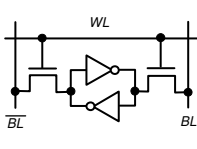
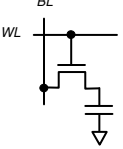
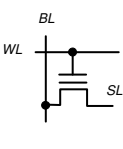
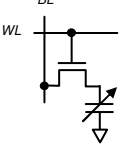
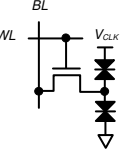
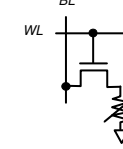
The Quest for Perfect Memory

An ideal memory should possess the following characteristics: (i) fast read/write time, (ii) high endurance, (iii) non-volatile, (iv) refresh free, (v) small in size, and (vi) low voltage operation [1]. In the VLSI era, there are several memory technologies that have been introduced, such as static random access memory (SRAM), dynamic random access memory (DRAM), and flash memory. In the last few years, there is a renewed interest in the development of magnetic RAM due to recent discoveries on magnetic phenomenon in nanoscale structure. In Table 1, the MRAM technology is compared to other memory architectures in terms of relative performances.

SRAM has fast read/write time, however requires a large area for each cell that has 4 transistors. DRAM occupies a small area but it has to be refreshed every few milliseconds. Flash has the advantage of being small and non-volatile, but the write time is very slow and the endurance is low compared to other types of memory. In other words, all the existing memory technologies in the market today do not have all the characteristics of an ultimate universal memory: fast read and write time, non-volatile, high endurance, refresh-free, small cell size, and low power operation [1,2]. As a result, modern electronic devices usually have to use two or more types of memories. For example, cell phones today require both a Flash and SRAM chip. To save cost and area, some manufacturers are using combination memories, where Flash and SRAM chips are stacked in a single package.

Tunnel diode based memory utilizes the inherent properties of quantum tunnelling, exhibiting fast write and read time, refresh-free, and low voltage. These characteristics make this memory technology to be a prime candidate for future memory applications. However, tunneling SRAM suffers from high power consumption due to constant standby power to retain the memory. On the other hand, MRAM seems to have superior performance in almost all categories. Therefore, it is sought to be the closest solution to the “perfect” memory.

Table 1. Comparison of different solid-state memory technologies. Bold typed features indicate undesirable characteristics.

Performance Categories	SRAM	DRAM	FLASH	FRAM	TSRAM	MRAM
Read time	Fast	Mod.	Fast	Mod.	Fast	Fast
Write time	Fast	Mod.	Slow	Mod.	Fast	Fast
Non-volatile	No	No	Yes	Yes	No	Yes
Endurance	Unlimited	Unlimited	Limited	Limited	Unlimited	Unlimited
Refresh	No	Yes	No	No	No	No
Cell Size	Large	Small	Small	Medium	Medium	Small
Low Voltage	Yes	Limited	No	Limited	Yes	Yes
Circuit Diagram						

For continued growth in memory products it will be essential to further scale the existing memory devices. As the memory elements get smaller, the memory state can be altered undesirably by thermal agitation posing challenges to scaling. It is questionable whether a stable SRAM cell can be scaled to the 32nm node without sacrificing cell size. Similarly, DRAM is

facing problems in how to store the required number of electrons in ever-diminishing storage volumes. For traditional non-volatile memory devices like NOR flash, scaling could stop even before the 32nm node, while scaling of mass storage devices like NAND flash, is going to be very difficult beyond the 32nm node. Novel architectures may be needed to further improve data bandwidth in embedded as well as stand-alone memory applications. As always, density and cost are important issues for memory devices. Solutions like 3D integration and stacking are viable alternatives to scaling. In order to realize stacked memory devices novel selection devices are needed [3].

SILICON BASED TUNNEL DIODE

The tunnel diode was first discovered by Esaki by fabricating Ge alloyed junction p-n diodes [4]. Unlike standard p-n junction diodes, the Esaki diode was degenerately doped on both sides of the metallurgical junction. He observed that the device exhibited a negative differential resistance (NDR) behavior due to band-to-band quantum-mechanical tunneling between electrons in the conduction band of the n+ materials tunnel through the bandgap to the valence band of the p+ material. However, fabrication via alloying fell out of favor following the invention of the integrated circuit.

The advancement of epitaxial growth techniques in the 1960's and 1970's resulted in the development of the resonant tunneling diode (RTD). Negative differential resistance in an RTD results when an electron tunnels to a resonant energy state in a quantum well. If the device is biased beyond the resonant energy, the tunneling probability becomes zero. The current drop results in NDR behavior. Unfortunately, this approach works well with III-V compound semiconductor materials but not with Si-based materials. Unlike III-V's, very few materials result in a large Si conduction band offset concurrent with a crystalline structure.

In 1993, Sweeny and Xu proposed a hybrid structure between the Esaki and RTD by incorporating δ -doping planes to create resonant states on both sides of the p-n junction and

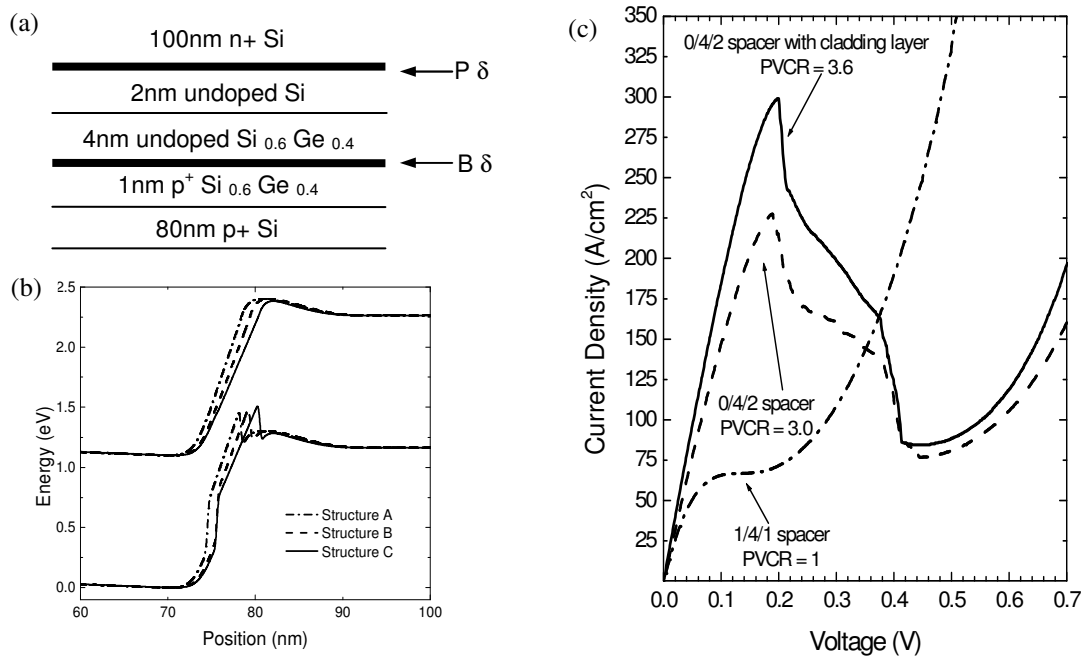


Fig. 1: (a) Schematic drawing of Si/SiGe RITD layers grown via LT-MBE. (b) The energy bands diagram of Si/SiGe RITD (c) A typical I-V characteristic of RITD, exhibiting PVCR up to 3.6 and J_p of 300 A/cm². [8]

enhance the dopant degeneracy [5]. In 1998, Rommel *et al.* was effectively the first to build Si-based resonant interband tunnel diode (RITD) using low-thermal Molecular Beam Epitaxy (LT-MBE) technique. Post growth rapid thermal anneal (RTA) was introduced to activate the dopant as well as to reduce point defects. Initial results showed PVCR of 1.54, and upon further lowering of the substrate temperature during MBE growth it improved to 2.05 [6,7]. Jin *et al.* continued the effort by replacing Sb with P to create δ -doping plane, which allows enhanced degeneracy due to higher solid solubility limit of P in the Si at the growth temperature. The latest proposed structure utilizes undoped SiGe layers to sandwich B δ -doping plane, suppressing the B diffusion during post-growth RTA. These modifications result in PVCR up to 3.6 and J_p of 300 A/cm² as shown in Fig. 1 [8]. Other research groups have also replicated Rommel's first proposed design. They have reported PVCR as high as 6, the present world record [9].

Tunneling-Based Static Random Access Memory

A memory architecture utilizing tunnel diode was first proposed by Goto *et al.* [10] and further advanced by Van der Wagt [11]. Each cell consists of two tunnel diodes connected in series with a current regulator, usually a FET, connected into the middle node. Fig. 2 illustrates the circuit diagram of the T-SRAM. The bottom tunnel diode acts as the driver, and the upper one function as a static load. By applying a bias onto V_{CLK} , a folded current-voltage characteristic is established. The intersections between the drive and load curves indicate the possible latching points. It is important to note at this point, that the intersection at the negative differential resistance (NDR) region is unstable and cannot be used as a latching point. Thus, in this particular case, the memory cell can either latch into the V_H or V_L , which can be regarded as **1** or **0**, respectively.

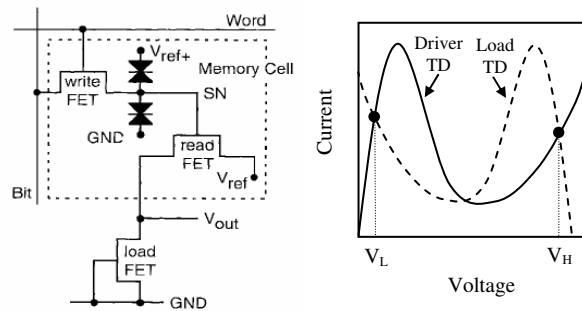


Fig. 2: The circuit diagram of T-SRAM and its typical I-V characteristics [11].

The latching from **0** to **1** occurs when the FET temporarily injects a current into the sense node, effectively shifting down the driver I-V characteristic. The shifting has to be substantial enough that the peak of the driver falls below the load characteristics. As a result, there is only one possible latching point that is at region higher than the driver peak voltage. Once the FET is turned off, the latching point will move to V_H and stay there unless the standby power is shut off. In the similar manner, the latching from 1 to 0 occurs when the FET temporarily acts as a current sink, shifting up the driver I-V characteristics. The demonstrations of this particular memory cell in III-V systems have been reported in the literature [12, 13].

The inherently fast tunneling phenomenon makes this type of memory architecture attractive. Combined with the possibility of vertical integration of the tunnel diode atop of the source/drain region of the FET, a compact design can be achieved. The claim to fame when first type of T-SRAM was proposed was that it may have the speed of the conventional SRAM at the footprint of DRAM.

The first successful demonstration of fully integrated T-SRAM in silicon platform was reported by Morimoto *et al.* [14]. The advancement, however, suffers from lack of ability to scale down the device dimension as well as the current densities. In June 2003, Si/SiGe RITDs, a more versatile device design in terms of dimension and current scalability, were successfully integrated with CMOS by the authors. The tunnel diodes were grown after all the high-temperature CMOS process steps through openings in low-temperature oxide layer. The integrated RITDs exhibit PVCR up to 2.8 with J_p of 260 A/cm² as shown in Fig. 3(a). A simple latch was also constructed

by utilizing a pair of tunnel diodes in series. Employing a FET to modulate current injection into the latch, a RITD/NMOS monostable-bistable transition logic element (MOBILE) was realized. Fig. 3(b) shows the characteristic of the latch, exhibiting 84% voltage swing between the on and off-state at a low applied clock voltage at 0.5 V [15].

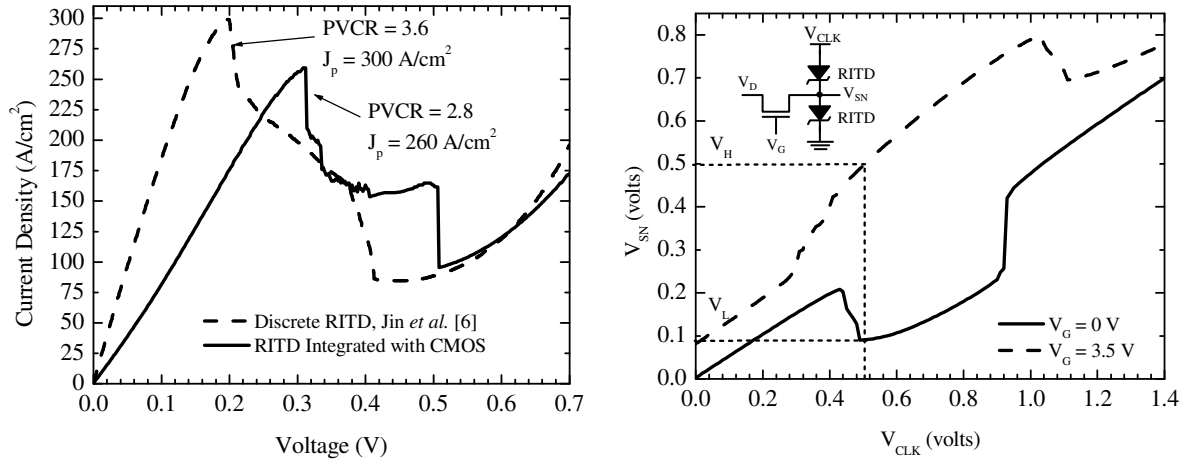


Fig. 3: (a) Current-Voltage characteristics of a monolithically integration Si/SiGe RITD on CMOS platform, and (b) Tunnel diode-based MOBILE latch [15]

MAGNETIC TUNNEL JUNCTION

The development of magnetic memory can be traced back to the early 1960s when the concept of non-volatile ferrite core memory was developed [16]. A great deal of effort was directed towards the development of thin-film magnetic memory, in which the storage cell comprises of a multilayered magnetic structure that can have different resistance values depending upon their states of magnetization. The major breakthrough for magnetic memory technology is the discovery of the giant magnetoresistance (GMR) effect first observed by Baibich *et al.* [17].

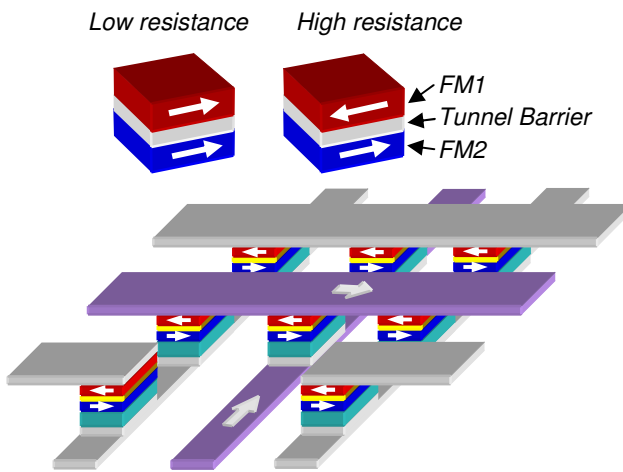


Fig. 4: A typical MTJs in array configuration.

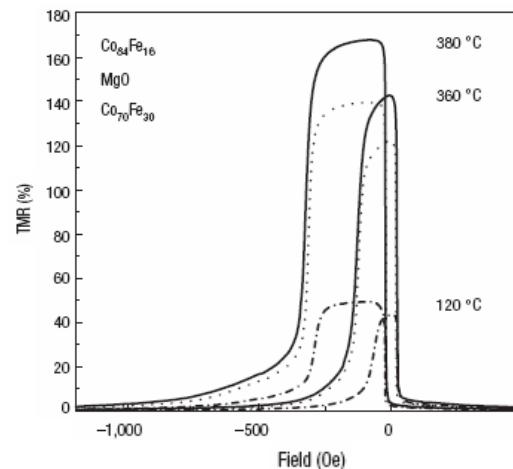


Fig. 5: The giant magnetoresistance change in TMR on CoFe/Mg-O/CoFe MTJ [21].

The discovery of GMR led to the construction of spinvalve sandwiches and magnetic tunnel junctions (MTJ). The basic structure of the magnetic spinvalve consists of two ferromagnetic (FM) layers separated by a non-ferromagnetic metallic layer. The magnetic orientation of the bottom FM layer is pinned in one particular direction by exchange coupling with the underlying antiferromagnetic layer (AF), while the magnetization of the upper FM layer is freely controlled by inducing an external magnetic field. Although in comparison to GMR multilayer structure the spinvalve has substantially lower saturation field with a reasonable MR ratio at room temperature [18, 19], they are still not suitable for memory applications.

MTJ, on the other hand, exhibits significantly lower switching fields (much less than 100 Oe [18]) with lower MR ratios at room temperature. A typical MTJ consists of two FM layers separated by a thin tunnel barrier, commonly made of Al-O material. The current in MTJ flows perpendicular to the film plane and is governed by spin-dependent tunneling. Fig. 4 illustrate typical configuration of MTJ in an array form. In ferromagnet, current is carried independently by spin up and spin down electrons in the conduction band. When the magnetization of FM layers is parallel to one another, there are equal densities of states for the spin-up electrons on both sides of the tunnel barrier. Maximum tunneling will occur and conductance will be at its maximum. On the other hand, when they are anti-parallel to one another, there are not enough states in the FM2 for the spin-up electrons in FM1 to tunnel to; thus, conductance decreases. This phenomenon gives rise to the magnetoresistance effect, with the highest reported to date of about 60% with Al-O [20] and 230% with Mg-O as tunnel barrier at room temperature [21, 22] as shown in Fig. 5. Table 2 lists various MTJ structures that have been fabricated and reported in the literature.

Table 2. Characteristics of selected MTJs.

MTJ	MR (%)	T (K)	H _S (Oe)	Method
Fe/Ge/Co	14	4.2	n/a	n/a [35]
Fe/Al ₂ O ₃ /Fe	18	RT	~52	Sputt. [36]
Co _{0.84} Fe _{0.16} /Al-O/Co _{0.84} Fe _{0.16}	40	RT	~25	Sputt. [37]
Co _{0.75} Fe _{0.25} /Al-O/Co _{0.75} Fe _{0.25}	50	RT	~25	Sputt. [38]
Co _{0.70} Fe _{0.30} /Al-O/Co _{0.70} Fe _{0.30}	60	RT	n/a	Sputt. [39]
Fe/MgO/Fe	180	RT	~25	Epitaxy[40]
Co ₈₄ Fe ₁₆ /MgO/Co ₇₀ Fe ₃₀	220	RT	~25	Sputt. [41]
CoFeB/MgO/CoFeB	230	RT	~25	Sputt. [42]

Magnetic Random Access Memory

A memory cell of 4-Mb MRAM that utilized a transistor and a MTJ was recently built by Freescale [23]. This is the largest MRAM demonstration to date that has been integrated with CMOS using copper interconnect technology. Although the achievement was very significant, the fabrication of the MRAM cell was very complex, involving multiple via and metallization steps in addition to of the already complex CMOS steps. Regardless of the complexity involved in fabrication, MTJ based MRAM has been sought to be a potential solution to the quest for the ultimate memory. Like T-SRAM, it has the potential to operate as fast as SRAM, have cell size as small as DRAM, operate at low voltage, and most important of all non-volatile.

QUANTUM AND SPIN BASED MRAM

A novel memory device can be constructed by integrating tunnel diode and magnetic tunnel junction. The MTJ will be vertically integrated on top of the RITD, adding no area to the cell

size. Figs. 6(a) and (b) show the schematic drawing of the structure and the circuit diagram in cross-point architecture.

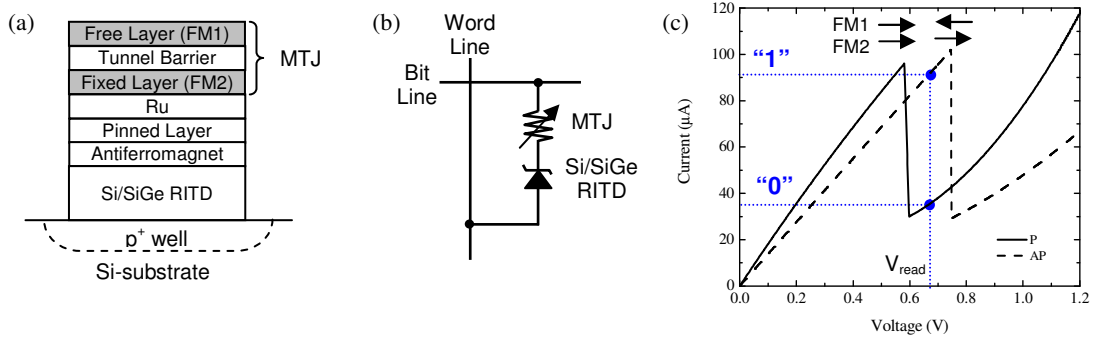


Fig. 6: Vertical integration of Si/SiGe RITD with MTJ.

By stacking a MTJ on top of a RITD, the MTJ becomes simply a variable resistor connected in series with the RITD. The solid curve on Fig. 6(c) represents the simulated I-V characteristics of the cell when both the magnetization of FM1 and FM2 are in parallel. The resistance of MTJ increases as the direction of magnetization of FM1 and FM2 become anti-parallel. The change in magnetoresistance causes a shift in the I-V curve of the tunnel diode, shown as the dashed line in Fig. 6(c). By properly biasing the device at a particular read voltage (V_{read}), the relatively small MR shift can be translated into a large current shift that is proportional to the PVCR of the tunnel diode. The measured current will determine the state of logic high and low.

In addition, enhancement in the MR ratio is also expected when the change in resistance is plotted against the applied magnetic field. The proof of concept that tunnel diodes can be used to enhance the MR ratio has been reported recently. Eumura *et al* bread boarded a p^+n^+ GaAs Esaki diode and CoFe-AlO_x-CoFe MTJ in a parallel configuration [24]. They observed a significant enhancement of the MR ratio by about 10 folds, from 11% to 103%. In a more recent study, their group also reported a huge MR ratio enhancement of 59 folds, from 15% to 890%, by putting a MTJ in series to the tunnel diode [25].

A multiple valued MRAM cell can be constructed by utilizing a multi-barrier MTJ. The bottom FM3 is pinned to an antiferromagnetic layer (AF), leaving FM2 and the upper FM1 as free layers. FM2 is chosen to have a coercive field higher than FM1. With two free FM layers and one fixed layer, as shown in Fig. 7(a), there are four different combinations of magnetization configurations. Each configuration will have different resistance values associated with it. As first suggested by Uemura *et al* [26], this structure can be harnessed to construct a four-valued MRAM based on binary logic computing.

Fig. 7(b) shows the simulated current-voltage characteristics of the proposed Si-SiGe RITD/MTJ four-valued MRAM using a cross-point architecture. Uemura *et al* also propose a novel read operation. The state **0**, **1**, **2**, and **3** can be represented in 2-bit binary forms as **00**, **01**, **10**, and **11**, respectively. To determine the first digit of the binary state, read voltage is chose to be in between peak voltage 2 (V_{P2}) and V_{P3} (point A). If the current is low then the first digit is **0**, otherwise is **1**. If the first state is **0** then the next read voltage will be between V_{P1} and V_{P2} (point B). If the first state is **1** then the next read voltage will be between V_{P3} and V_{P4} (point C). To determine the second digit of binary state, the same condition is applied. If the sensed current is low then the second digit is **0**, otherwise is **1**. Thus, the state of the memory cell can be known by using two read voltages [26].

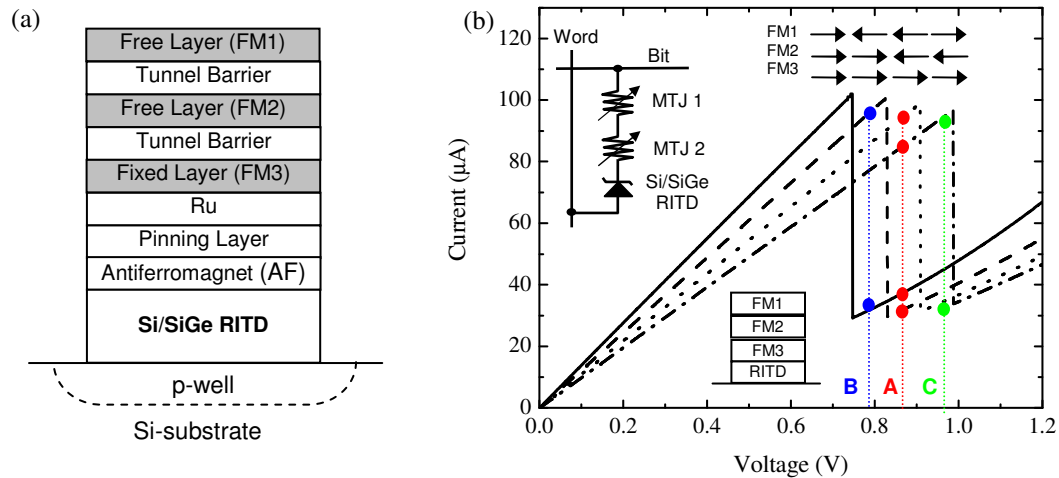


Fig. 7: (a) Double barrier MTJ. (b) Simulated results of I-V characteristics of four value Si/SiGe RITD/MTJ MRAM cell.

SUMMARY

A review of advances in resonant tunnel diodes has been provided. Silicon based resonant interband tunnel diodes show promise for applications in next generation memory devices due to their fast read-write responses that rely on quantum tunneling and their compatibility with CMOS. It has been shown that when combined with spin based magnetic tunnel devices, tunnelling magnetoresistive multivalued non-volatile memory elements can be constructed. The challenges of integration and scaling remain to be solved for making it a viable technology.

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