Overgrown Si/SiGe Resonant Interband Tunnel Diodes for Integration with CMOS

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The incorporation of tunnel diodes with field effect transistors (FET) can improve the speed and power capability in electronic circuitry. This has been realized in III-V materials by demonstrating a low power refresh-free tunneling-SRAM [1] and high performance compact A/D converter [2]. A new thrust to integrate tunnel diodes with the mainstream CMOS technology led to the invention of Si/SiGe resonant interband tunnel diode (RITD) [3] with the highest reported peak-to-valley current ratio (PVCR) of 6.0 [4]. The structure consists of a SiGe spacer *i*-layer sandwiched between two delta-doped planes grown by Low-Thermal Molecular Beam Epitaxy (LT-MBE) [5]. By adjusting the spacer layer thickness, the peak current density (J_p) can be adjusted from 0.1 A/cm^2 up to 151 kA/cm^2 [6]. Recently, monolithic integration of RITD with CMOS has been realized, demonstrating a low-voltage operation of a monostable-bistable logic element (MOBILE) [7].

In this study, RITD layers were grown through openings in a 300 nm thick chemical vapor deposition (CVD) SiO_2 layer. Traditionally, a mesa etch step patterns the active device area within the oxide opening; it is known as the patterned growth approach, Fig. 1(a). However, this is not scalable for sub-100 nm oxide openings due to stringent alignment requirements. In this study, an alternative scheme has been investigated by defining a mesa that was larger than the oxide opening as illustrated in Fig. 1(b). Thus, part of the film grown on top of the oxide was intentionally included to be part of the device. This type of device is referred to as an overgrown RITD. A mesa etch was carried out using a gas mixture of SF_6 and He, followed by rapid thermal annealing at 825^{o}C for 1 min. in N_2.

The SEM micrograph in Fig. 2 shows a cross-section of the overgrown RITD at the Si/SiO_2 interface. The film grown on top of the oxide shows a polycrystalline structure with a very fine grain size. On the other hand, the film grown on top of the p^+substrate has a crystalline structure. Therefore, the epitaxial formation only occurs in the region defined by the oxide opening where the crystalline substrate is exposed. In addition, the transition region from poly-to-crystalline is found to be both abrupt, substantially less than 20 nm, and vertical, which is highly desirable for scaling the device size down in lateral dimension.

Fig. 3 illustrates the current-voltage (I-V) characteristics of a 25×25 μm^2 patterned growth RITD and an overgrown RITD with a mesa size of 37×37 μm^2 on 31×31 μm^2 oxide opening. The patterned growth tunnel diode results in a PVCR of 3.13 with a peak current (I_p) of 8.3 mA, and the overgrown RITD yields a PVCR of 2.50 with I_p of 13.0 mA. While the device area of the patterned growth tunnel diode is the mesa size, the effective active area of the overgrown structure is less obvious. Based on the SEM analysis, it is hypothesized that the oxide opening defines the diode active area. This assumption is confirmed by the fact that when the electrical data is normalized to the device area, the J_p of patterned growth and overgrown RITD are comparable at 1.30 kA/cm^2 and 1.35 kA/cm^2, respectively.

In conclusion, overgrown RITDs can conceivably be integrated with advanced CMOS devices through contact cut openings in the source and drain as shown in Fig. 5. The fabrication will require a maximum of two additional mask steps to alternately grow tunnel diodes on PMOS and NMOS. The diode electrical area is defined by the size of the contact cut openings. The SEM analysis suggests that the lateral size of the tunnel diode can be scaled down to 100 nm due to the abrupt nature of the poly-to-crystalline transitional region.

REFERENCES

[1] J. P. van der Wagt, A. C. Seabaugh, and E. Beam, "RTD/HFET Low Standby Power SRAM Gain Cell," *IEEE Elec. Dev. Lett*, vol. 19, pp. 7-9, 1998.
[2] T. Broekaert, B. Brar, J. P. van der Wagt, A. Seabaugh, F. Morris, T. Moise, E. Beam, and G. Frazier, "A Monolithic 4-bit 2-gsps Resonant Tunneling Analog-to-Digital Converter," *IEEE J. Solid-State Circ.*, vol. 33, pp. 1342-1349, 1998.
[3] S.L. Rommel, T.E. Dillon, M.W. Dashiell, H. Feng, J. Kolodzey, P.R. Berger, P.E. Thompson, K.D. Hobart, R. Lake, A.C. Seabaugh, G. Klimeck, and D.K. Blanks, "Room Temperature Operation of Epitaxially Grown Si/$Si_{0.5}Ge_{0.5}$/Si Resonant Interband Tunneling Diodes," *Appl. Phys. Lett.*, vol. 73, pp. 2191-93, 1998.
[4] K. Eberl, R. Duschl, O.G. Schmidt, U. Denker, and R. Haug, "Si-Based Resonant Inter- and Intraband Tunneling Diodes," *Journal of Crystal Growth*, 227-228, pp. 770-76, 2001.

[5] N. Jin, S.Y. Chung, A.T. Rice, P.R. Berger, R. Yu, P.E. Thompson, C. Rivas, R. Lake, S. Sudirgo, J.J. Kempisty, B. Curanovic, S.L. Rommel, K.D. Hirschman, S.K. Kurinec, P.H. Chi, and D.S. Simons, "Diffusion Barrier Cladding in Si/SiGe Resonant Interband Tunneling Diodes and Their Patterned Growth on PMOS Source/Drain Regions," *IEEE Trans. Elec. Dev.*, vol. 50, pp. 1876-1884, 2003.

[6] N. Jin, S.Y. Chung, A.T. Rice, P.R. Berger, R. Yu, P.E. Thompson, R. Lake, "151 kA/cm^2 Peak Current Densities in Si/SiGe Resonant Interband Tunneling Diodes for High Power Mixed-Signal Applications," *App. Phys. Lett.*, 83, pp. 3308-3310, 2003.

[7] S.Sudirgo, R.P. Nandgaonkar, B. Curanovic, J. Hebding, R. Saxer, K.D. Hirschman, S.S. Islam, S.L. Rommel, S.K. Kurinec, P.E. Thompson, N. Jin, and P.R. Berger, "Monolithically Integrated Si/SiGe Resonant Interband Tunnel Diode (RTD)/CMOS Demonstrating Low Voltage MOBILE Operation," *Proceedings on 2003 International Semiconductor Device Research Symposium*, pp. 22, 2003.

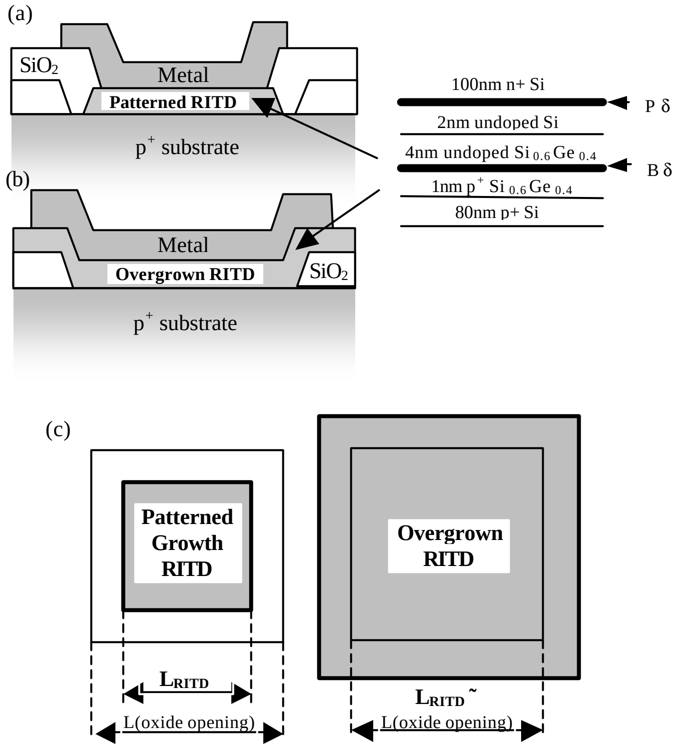

Fig. 1. (a) Cross-sectional diagram of patterned growth RITD, (b) overgrown RITD, and (c) top view diagrams of patterned growth and overgrown RITD.

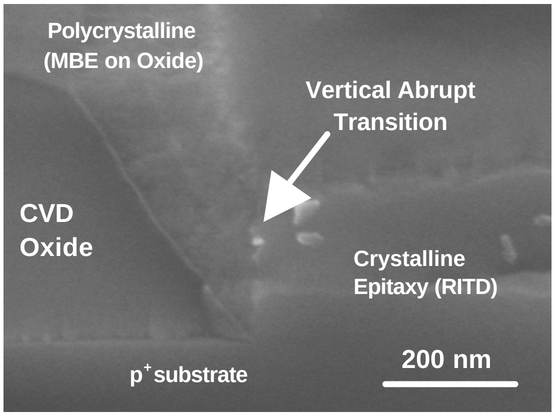

Fig. 2. SEM micrograph of the overgrowth RITD on the Si/SiO$_2$ interface.

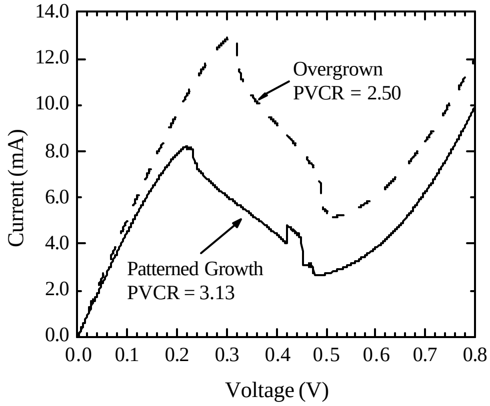

Fig. 3. I-V characteristics of $25\times25\ \mu m^2$ patterned growth and $37\times37\ \mu m^2$ mesa/ $31\times31\ \mu m^2$ oxide opening overgrowth RITD.

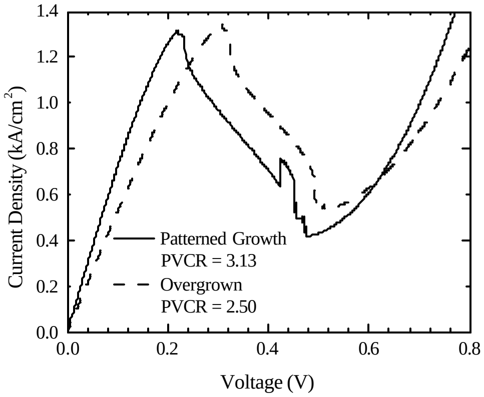

Fig. 4. Normalized I-V characteristics based on the assumption that the effective area of the overgrowth RITD is approximately equal to the area of oxide opening.

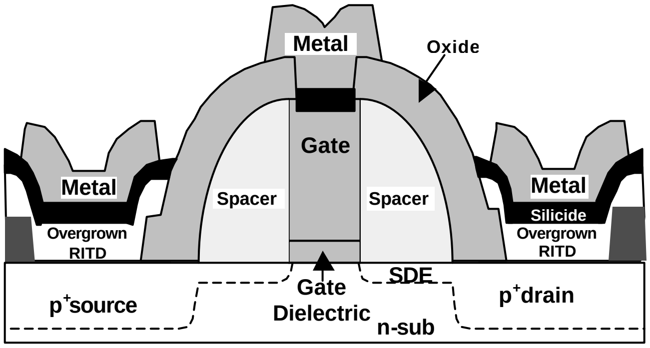

Fig. 5. Schematic drawing of two overgrown RITDs directly integrated on top of source/drain of a PMOS.