Student Paper

Monolithically Integrated Si/SiGe Resonant Interband Tunneling Diodes/CMOS MOBILE Latch with High Voltage Swing

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RTD-FET circuits in III-V materials have demonstrated improved speed and power capability in circuits such as ultra-low power tunneling-SRAM [1], as well as logic applications such as multiplexers [2] and analog-to-digital converters [3]. Recent breakthroughs in the development of Si/SiGe RITDs using molecular beam epitaxy (MBE) [4] have produced discrete RITDs with peak-to-valley current ratio (PVCR) up to 6.0 [5], and peak current density (J_p) as high as 151 kA/cm^2 [6]. Fig. 1 shows the latest variation of the RITD structure used as the control growth template in this study [7]. It features a SiGe *i*-layer sandwiched between two δ-doping injectors to enhance degeneracy, creating quantum wells at both sides of the tunnel diode. Discrete devices with this structure typically exhibit a PVCR of 3.6 and J_p of 0.3 kA/cm^2 [7]. The integration with CMOS requires that RITDs to be grown through patterned oxide openings on implanted regions. Prior study by the authors showed that the selective growth process and the propagation of residual implant damage into the RITD layers resulted in lower PVCR, ranging from 2.4 to 3.3 [8].

A comparatively relaxed CMOS process was used for integration feasibility studies that addressed the key challenges and enabled rapid turnaround. The process included (1) twin-well technology, (2) localized oxidation on silicon (LOCOS) for isolation, (3) 37 nm SiO_2 gate dielectric, (4) heavily n-doped polysilicon gate, (5) self-aligned source and drain formation, and (6) Al(1%Si) for contact and metallization. Based on thermal budget considerations, the strategy employed was to integrate the RITD after the high temperature front-end steps, up to the source/drain formation, but prior to metallization. The RITD structures were selectively grown on p+ regions created for the source/drain of the PMOS. The devices were annealed using rapid thermal anneal (RTA) at 825^{o}C for 1 min to reduce point defects formed during the low temperature MBE growth process. The tunnel diodes were patterned using dry etch technique in SF_6 and He gas mixture (Fig. 2).

Figs. 3 and 4 show the electrical characteristics of a monolithically integrated CMOS/RITD devices. Typical I_D-V_D characteristics of the NMOS and PMOS transistors, with L_{eff} of 1.5 μm, are shown in Fig.3. A 25×25 μm^2 Si/SiGe RITD grown in the same die exhibits negative differential resistance (NDR) behavior with a PVCR of 2.8 and a J_p of 0.26 kA/cm^2 (Fig. 4).

A monostable-bistable transition logic element (MOBILE) was realized using a pair of 25×25 μm^2 RITD in series as shown in the inset of Fig. 5. RITD1 and RITD2 functioned as the drive and load, respectively. An NMOS was used as a current injector into the sense node. While varying the clock voltage (V_{CLK}), the voltage at the sense node (V_{SN}) was measured when the NMOS was off (i.e. V_G = 0 V) and on (i.e. V_G = 3.5 V). At a given V_{CLK}, the circuit latches to two different operating voltages, exhibiting bistability. Moreover, the circuit shows high voltage swing, $\Delta V = V_H - V_L$, of 84% of the applied clock voltage at 0.5 V. This result also indicates that RITD-NMOS MOBILE latch is suitable for low-voltage operation.

In conclusion, Si/SiGe RITDs grown by MBE have been monolithically integrated with CMOS for the first time. The integrated devices resulted in a PVCR of 2.8 at room temperature, showing promise towards the realization of RITD/CMOS circuitry. A RITD-NMOS MOBILE latch has been demonstrated in Si. This logic element enables digital and ternary circuit design for high density storage.

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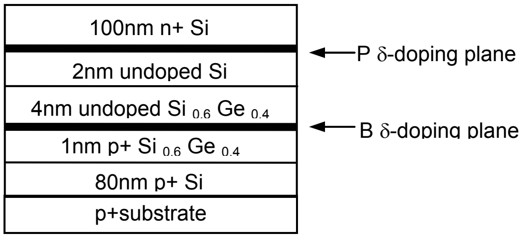

Fig 1. Schematic Diagram of the Si/SiGe RITD [7].

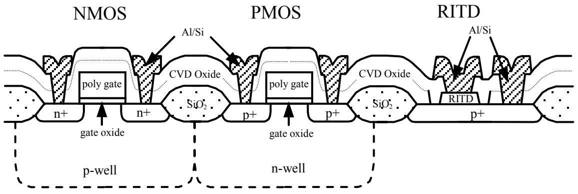

Fig 2. Schematic Diagram of the monolithically integrated CMOS and Si/SiGe RITD.

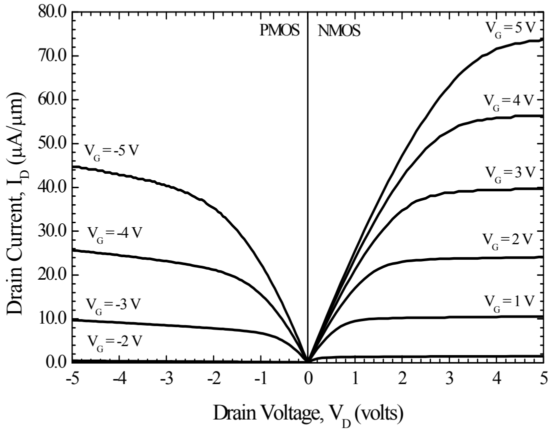

Fig 3. I_D-V_D characteristics of NMOS and PMOS, both with a L_{eff} =1.5 μm.

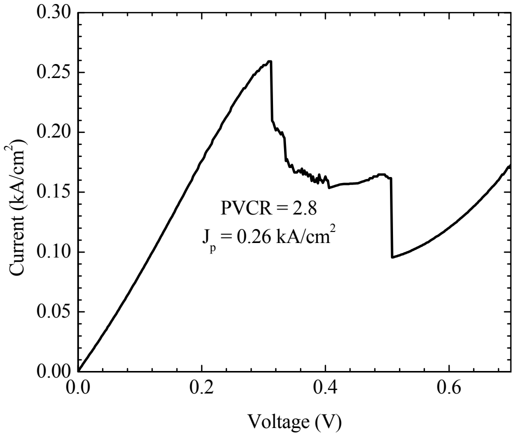

Fig 4. I-V characteristics of the first integrated 25x25 μm^2 patterned growth RITD. The RITD is in the same die as the CMOS devices plotted in Fig. 3.

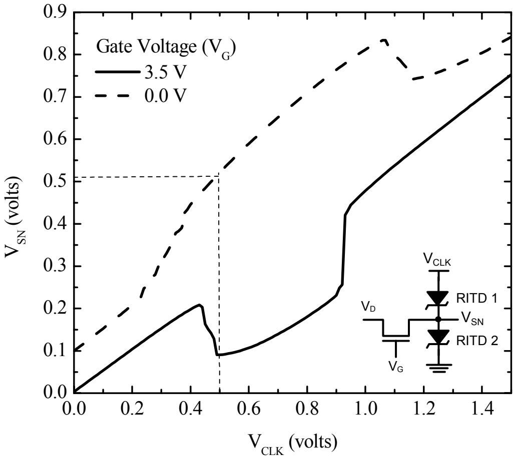

Fig 5. Voltage at sense node vs. supply voltage of a NMOS-RITDs Mobile Latch with 84% voltage swing of the applied V_{CLK} at 0.5 V.