

Challenges in Integration of Resonant Interband Tunnel Devices with CMOS

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Abstract—The fabrication of SiGe Resonant Interband Tunnel Devices (RITD) using CMOS compatible processes requires ability to form RITD structures selectively on source/drain regions. Various approaches were investigated and RITDs have been realized in lithographically defined openings in oxide on Si wafers. Patterned growth RITD on p+ Si exhibited a peak-to-valley current ratio (PVCr) of 3.0 and peak current density (J_p) of 188 A/cm² whereas RITD of p+ implanted regions resulted in a PVCr of 2.5 with J_p of 278 A/cm². Blanked growth RITD on p+ implanted substrate yielded a superior PVCr of 3.3 and J_p of 332 A/cm². The observed effects of patterned growth and implanted substrate on the RITD device performance are critical challenges addressed in this study for RITD-CMOS integration.

Index Terms—Resonant Interband Tunneling Diodes (RITD), Resonant Tunneling Devices, CMOS integration.

I. INTRODUCTION

THE tremendous growth in microelectronics industry has been fueled by the rigorous effort to downscale Complementary Metal Oxide Semiconductor (CMOS) device dimensions. Conventional CMOS device, however, will begin to meet challenging scaling efforts as it approaches gate linewidth of about 70 nanometers. The limitation is not due to the inability to shrink its physical dimension, but due to the degrading effect of quantum phenomena that begins to dominate the device operation [1], [2]. The International Technology Roadmap for Semiconductors (ITRS) predicted several emerging technologies that can provide near-term solutions, and one of these is the Resonant Tunnel Diodes–Field Effect Transistors (RTD-FET) technology [3]. Large scale integration of tunnel diodes with CMOS has potential to produce circuitry that exhibits higher circuit speed, reduced component count, and lowered power consumption, which will extend the CMOS on the ITRS roadmap without linewidth reduction.

Tunnel diodes current-voltage behavior exhibits negative differential resistance (NDR) often characterized by a figure

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of merit, the peak to valley current ratio (PVCr). Up to the early part of 1990s, most of the work in tunnel diode development was done in III-V compound semiconductors. Recent breakthrough in the development of Si-based RITD by Rommel *et al.*, however, showed a promising potential in overcoming the compatibilities issues. The structures investigated utilized undoped Si and SiGe spacer layers sandwiched between two δ -doping planes grown by MBE [4]. The device is fabricated using low temperature-molecular beam epitaxy (LT-MBE) to minimize dopant diffusion and segregation during growth. Superior performance has also been achieved by R. Duschl, *et al.* who have replicated this structure with a PVCr of 6 [5], [6]. Fig. 1 illustrates the latest variation to this discrete structure proposed by Jin *et al.* that exhibits PVCr as high as 3.6 with current peak density (J_p) of 0.2 kA/cm² [7]. This structure is used in this study for possible integration with CMOS technology.

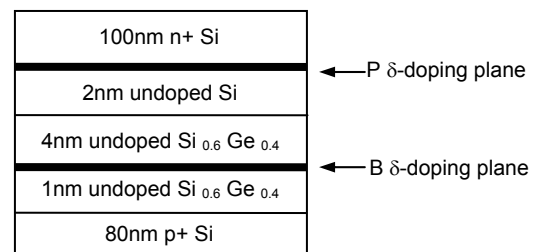


Fig. 1. Schematic diagram of RITD structure.

II. INTEGRATION STRATEGIES

Integration of Si-based tunnel diodes with CMOS will require some modifications to the existing CMOS fabrication steps. The goal is to minimize this impact and limit the number of steps in the process. Based on the thermal budget consideration of both devices as shown in Table I, a feasible integration approach is to grow the Si-based RITD onto a CMOS template following all front-end thermal processes, prior to metallization.

The most suitable place to build RITD was right on top of the source/drain (S/D) of CMOS devices. This configuration allows three-dimensional structuring where one device is integrated vertically on top of the other. There are many advantages to this strategy. First, compact circuitry that requires less area with greater functionality can be achieved. Secondly, there is possibility that S/D and RITD can be

TABLE I
THERMAL BUDGET OF CMOS AND RITD

CMOS		RITD	
Critical Steps	Temp(°C)	Critical Steps	Temp(°C)
Well drive-in	1100	MBE Growth	320-650
Field oxide growth	1100	Post-growth anneal	825
Gate oxide growth	1000		
Poly gate deposition	610		
S/D anneal	1000		
Passivation	425		
Metal sintering	415		

CMOS process is based on the p-well CMOS technology developed at Rochester Institute of Technology [8].

formed in a single MBE growth, featuring RITD on raised S/D stacks. In this study, RITDs were grown on regions, which have been implanted with identical condition as the S/D of PMOS as shown schematically in Fig. 2.

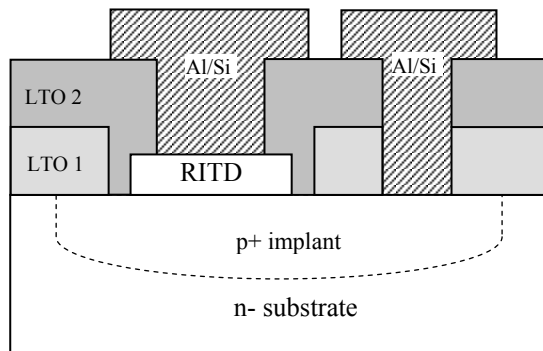


Fig. 2. Schematic diagram of patterned growth RITD structure through openings in CVD low temperature oxide (LTO)..

This scheme will require building RITD through openings in CVD low temperature oxide (LTO). In other words, CMOS compatibility requires that MBE layers are grown on a substrate with patterned oxide; hence, it is termed patterned growth in comparison to bulk growth in discrete tunnel diode fabrication. The presence of oxide imposes limitation to the substrate cleaning in preparation for epitaxial growth. The abbreviated Shiraki process [9] can no longer be used. Instead, the wafers were cleaned using a standard RCA clean process with a short HF treatment as the last step.

In addition, RITD structures also need to be grown atop of implanted regions. It is well investigated that dopant introduction through ion implantation causes lattice damage. Therefore, optimum annealing step is required to eliminate as many defects as possible.

Finally, the compatibility of the metal used for contacts are considered. Ti/Au that is used in the discrete devices are not appropriate for CMOS. In this study, aluminum doped with 1% silicon (Al/Si) is used. The use of silicide contacts will be a subject of future study.

III. EXPERIMENTAL DETAILS

A 500 nm-thick of thermal oxide was grown on n-type (100) Si-substrate at 1100°C in wet O₂. The oxide then was patterned using conventional lithography technique and etched in 10:1 HF solution. The oxide/resist stack then was used as implant mask during the formation of p+ S/D region. The wafers were implanted with boron (B11), 2×10^{15} , at 30 keV. The implant damage was annealed at 1000°C in N₂ for 20 min and wet O₂ for additional 10 min. All oxide on the sample was etched in 10:1 HF solution. RCA clean was carried out.

The next step was to deposit 300 nm-thick of LTO using Low Pressure Chemical Vapor Deposition (LPCVD) technique at 425°C. The areas where RITDs would be grown were lithographically defined, and the oxide was etched using 10:1 HF. RCA clean was performed again. To remove native oxide and ensure successful growth, the samples were introduced to dilute 50:1 HF for 40 sec prior to growth. Patterned growth then was carried out on the p+ S/D implanted regions using LT-MBE process.

Using conventional lithography process, RITD mesa structures were defined with different sizes ranging from 10 μm to 100 μm in diameter. The unwanted MBE then was removed using dry etch technique in the SF₆ plasma. A second layer of 300 nm-thick LTO was deposited. Contact cuts opening were then lithographically defined and etched using 10:1 HF. The resist was removed using O₂ plasma. Prior to metallization the wafers went through Ammonium Peroxide Mixture (APM) clean and 50:1 HF dip for 1 min. It is followed by the deposition of 600 nm thick of Al/Si by sputtering technique. Finally, the wafers were sintered at 420°C for 20 minutes in H₂/N₂ for better ohmic contact.

To investigate the influence of patterned growth and residual implant damage, various schemes were employed: 1) Patterned growth RITD on p+ substrate, 2) Bulk RITD on p+ implanted substrate, and 3) Patterned growth RITD on p+ implanted regions.

IV. RESULTS AND DISCUSSION

Fig. 3 shows the current-voltage (IV) curves of different structures investigated. All of the devices show NDR behavior. In the case of the first structure, patterned growth RITD on p+ substrate, the PVCR was 3.0 with J_p of 188 A/cm². The peak voltage is shifted to higher value than a typical tunnel diode due to higher series resistance observed in this device. Moreover, the second structure, bulk-growth RITD on p+ implanted substrate results in a PVCR of 3.3 and J_p of 332 A/cm². The peak voltage is within normal range. The valley current, however, is shown to be higher than devices built on p+ substrate. Lastly, the third structure, patterned growth RITD on p+ implanted regions shows about 15% reduction in peak current, resulting in lower PVCR of 2.5 and J_p of 278 A/cm². The valley current is slightly higher than the second structure but significantly higher than the first device.

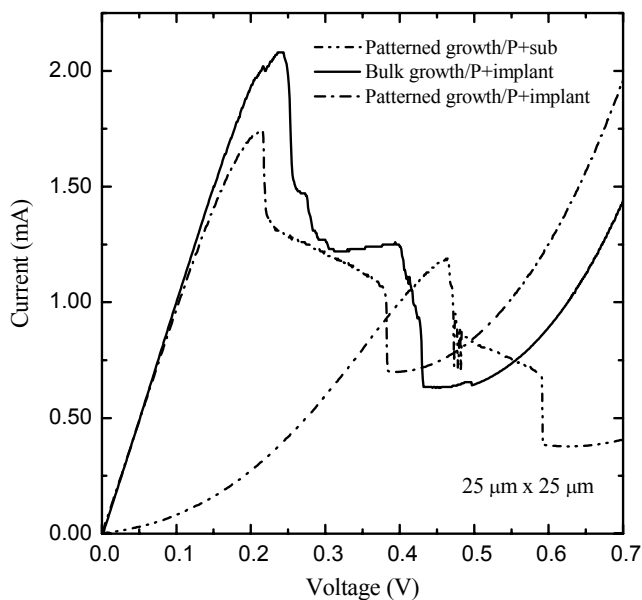


Fig. 3. RITD Current-Voltage characteristics of different structures.

Table I illustrates the cross-sections of the devices and their corresponding PVCr and J_p for each case. The results in this study was compared to the study reported by Jin et al. [4], which is bulk growth RITD on p+ substrate.

TABLE II
DEVICE STRUCTURE SCHEMATICS AND ELECTRICAL RESULTS

Substrate	MBE	Schematic	PVCr	J_p (A/cm ²)
P+wafer	Bulk		3.6*	200*
P+wafer $\rho = 0.012$ $\Omega\cdot\text{cm}$	Patterned		3.0	188
P+implant B11, $2 \times 10^{15} \text{ cm}^{-2}$, 30 keV	Bulk		3.3	332
P+implant B11, $2 \times 10^{15} \text{ cm}^{-2}$, 30 keV	Patterned		2.5	278

* Ref. [4]

Using Jin's result as the standard, the first structure shows the effect of patterned growth process. The reduction in PVCr can be attributed to the degradation in the crystal quality of the epitaxy layer. The MBE growth mechanism is largely dependent upon the surface diffusion of the arriving species on the substrate. The elevated substrate temperature supplies energy to the absorbed species to move around on the surface until a favorable lattice site is found where nucleation

begins. To grow a crystalline film, layer-by-layer growth is preferred. However, the presence of defect or abrupt edges, such as LTO/Si interface will most likely alter the growth process.

Given the nature of MBE growth, the epitaxial layers is expected to be crystalline on top of the Si surface and amorphous atop of LTO. Therefore, there may be a transitional region from amorphous to crystalline over the sidewall of oxide openings. The extension of this region into the actual device structure (i.e. where the mesa is defined) may degrade device performance.

Comparing the second structure to Jin's device, the effect of p+ implanted substrate on RITD performance was investigated. The reduction in PVCr can be attributed to the propagation of residual implant damage into the RITD structure. Inadequate annealing prior to MBE growth can leave end-of-range point defects that have tendency to propagate toward the surface during subsequent thermal process.

This conclusion is supported by a previous study. A sample wafer was implanted with BF_2 , $2 \times 10^{15} \text{ ions/cm}^2$, and at 150 keV. The sample was then annealed at 1000°C in N_2 for 20 minutes and in wet O_2 for 10 minutes. The oxide grown during the anneal process was etched away using hydrofluoric acid (HF) solution. RITD layers were grown and followed by post-growth anneal at 825°C for 1 minute. The sample was analyzed using TEM as shown in fig. 4. It is evident that residual implant damage propagates through RITD layers.

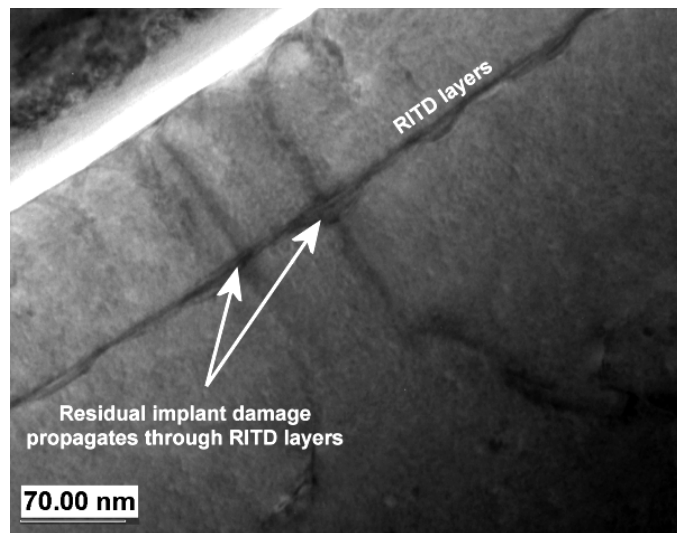


Fig. 4. Cross-section TEM micrograph of a RITD structure on an implanted p+ Si substrate.

Furthermore, it is also evident that the valley current on devices built on p+ implanted substrate generally exhibits higher valley current than the ones grown on p+ substrate. This is an indication of increased in the number of defect sites due to implantation, resulting in higher leakage current.

The third structure includes the patterned growth process and implanted regions. The substantial reduction in PVCR can be attributed to the combined effects of degree of crystallinity and implant damage causing increase in defect sites, resulting in higher leakage current.

V. CONCLUSION

In conclusion, Si based RITD devices have been realized for the first time in oxide openings and on implanted regions. Critical CMOS process integration challenges have been identified and discussed. Individual effect of patterned growth and end-of-range implant damage were observed, causing a slight reduction in device performance. When both processes were employed, the effects were coupled, resulting in substantial degradation in the electrical characteristics.

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REFERENCES

- [1] L. Geppert, "Quantum Transistors: Toward Nanoelectronics," *IEEE Spectrum*, Sept. 2000.
- [2] D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and H.P. Wong, "Device Scaling Limits of Si MOSFETs and Their Application Dependencies," *Proc. of the IEEE*, vol. 89, pp. 259-287, 2001.
- [3] *International Technology Roadmap for Semiconductors*, Semiconductor Industry Association (SIA), Austin, TX, 2001
- [4] S.L. Rommel, T.E. Dillon, M.W. Dashiell, H. Feng, J. Kolodzey, P.R. Berger, P.E. Thompson, K.D. Hobart, R. Lake, A.C. Seabaugh, G. Klimeck, and D.K. Blanks, "Room Temperature Operation of Epitaxially Grown Si/Si_{0.5}Ge_{0.5}/Si Resonant Interband Tunneling Diodes," *Appl. Phys. Lett.*, vol. 73, pp. 2191-93, 1998.
- [5] R. Duschl, O.G. Schmidt, C. Reitemann, E. Kasper, and K. Eberl, "High Room Temperature Peak-to-Valley Current Ratio in Si Based Esaki Diodes," *Electronics Letters*, vol. 35, pp. 1111-12, 1999.
- [6] R. Duschl, O.G. Schmidt, and K. Eberl, "Epitaxially Grown Si/SiGe Interband Tunneling Diodes with High Room-Temperature Peak-to-Valley Ratio," *App. Phys. Lett.*, vol. 76, pp. 879-81, 2000.
- [7] N. Jin, A.T. Rice, P.R. Berger, P.E. Thompson, P.H. Chi and D.S. Simons, "SiGe Diffusion Barriers for P-doped Si/SiGe Resonant Interband Tunnel Diodes", IEEE Proceeding, Lester Eastman Conference on High Performance Devices, 2002, pp. 265-269.
- [8] L. Fuller, "The manufacture of CMOS integrated circuit in a university microelectronics laboratory", *IEEE Thirteenth Biennial University/Government/Industry Microelectronics Symposium*, Minneapolis, MN, June 20-23, pp.211-215, 1999.
- [9] P.E. Thompson, M.E. Twigg, D.J. Godbey, K.D. Hobart, D.S. Simons, "Low-temperature Cleaning Processes for Si Molecular Beam Epitaxy", *J. Vac. Sci. Tech.*, pp. 1077-1082, May-Jun 1993.