Wafer-Scale Production of Uniform $InAs_yP_{1-y}$ Nanowire Array on Silicon for Heterogeneous Integration

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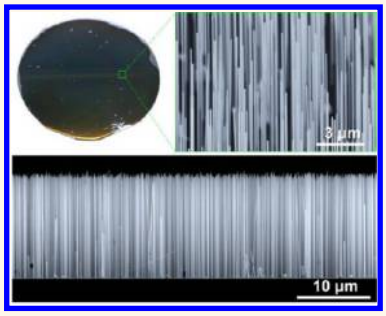
ABSTRACT One-dimensional crystal growth allows the epitaxial integration of compound semiconductors on silicon (Si), as the large lattice-mismatch strain arising from heterointerfaces can be laterally relieved. Here, we report the direct heteroepitaxial growth of a mixed anion ternary $InAs_yP_{1-y}$ nanowire array across an entire 2 in. Si wafer with unprecedented spatial, structural, and special uniformity across the entire 2 in. wafer and dramatic improvements in aspect ratio (>100) and area density (>5 × 10^8/cm^2). Heterojunction solar cells consisting of n-type $InAs_yP_{1-y}$ ($y = 0.75$) and p-type Si achieve a conversion efficiency of 3.6% under air mass 1.5 illumination. This work demonstrates the potential for large-scale production of these nanowires for heterogeneous integration of optoelectronic devices.



KEYWORDS: MOCVD · $InAs_yP_{1-y}$ · nanowire · III−V semiconductor · heterojunction

High-aspect-ratio semiconductors have led to significant breakthroughs in conventional electrical, optical, and energy-harvesting devices.[1−4] Among such structures, III−V semiconductor nanowires offer unique properties arising from their high electron mobility and absorption coefficients, as well as their direct band gaps.[1,5−8] Moreover, III−V semiconductors can tune their band-gap energy by formation of ternary or quaternary alloys.[9] For example, $In_xGa_{1-x}As$ or $InAs_yP_{1-y}$ can cover a band-gap energy range of over 1 eV (*i.e.*, 0.35−1.4 eV), allowing for enormous improvement in the performance of optoelectronic devices by formation of heterojunctions (*e.g.*, quantum well lasers and tandem solar cells). The vapor−liquid−solid (VLS) method, which facilitates one-dimensional (1-D) crystal growth of semiconductors using metal catalysts, has been widely used to synthesize III−V semiconductor nanowires.[10,11] However, metal-induced contamination presents a serious concern because metal atoms from the catalyst can create deep trap levels in the semiconductor band gap, which degrade the device performance.[12−14] Furthermore, ternary nanowires grown using metal catalysts suffer from a large gradient of alloy compositions along the nanowire length.[9,15−17] Even self-catalyzed (*i.e.*, gallium (Ga)-assisted) ternary nanowires present a large composition gradient, as observed by X-ray diffraction (XRD) and energy-dispersive X-ray spectroscopy (EDX) analyses.[18] Selective-area epitaxy (SAE) is another well-known method for the growth of III−V semiconductor nanowires.[1,19,20] For the SAE approach, nanosized hole patterns are fabricated *via* electron (e)-beam lithography, which is very time-consuming and thus limits pattern area.[6] Novel patterning methods, including nanosphere lithography[21,22] and diblock copolymer lithgraphy,[23] have shown promise for producing wafer-scale high-density growth of III−V quantum dots. Note that Si is the most universal platform for the electronics industry; therefore epitaxial integration of III−V on Si provides an active optic system with CMOS technology.[24,25] Catalyst-free, self-assembled growth of ternary $In_xGa_{1-x}As$ nanowires has recently been demonstrated on Si substrates.[26] The lattice-mismatch strain between Si and $In_xGa_{1-x}As$ allows 1-D crystal growth on Si without pattern assistance.

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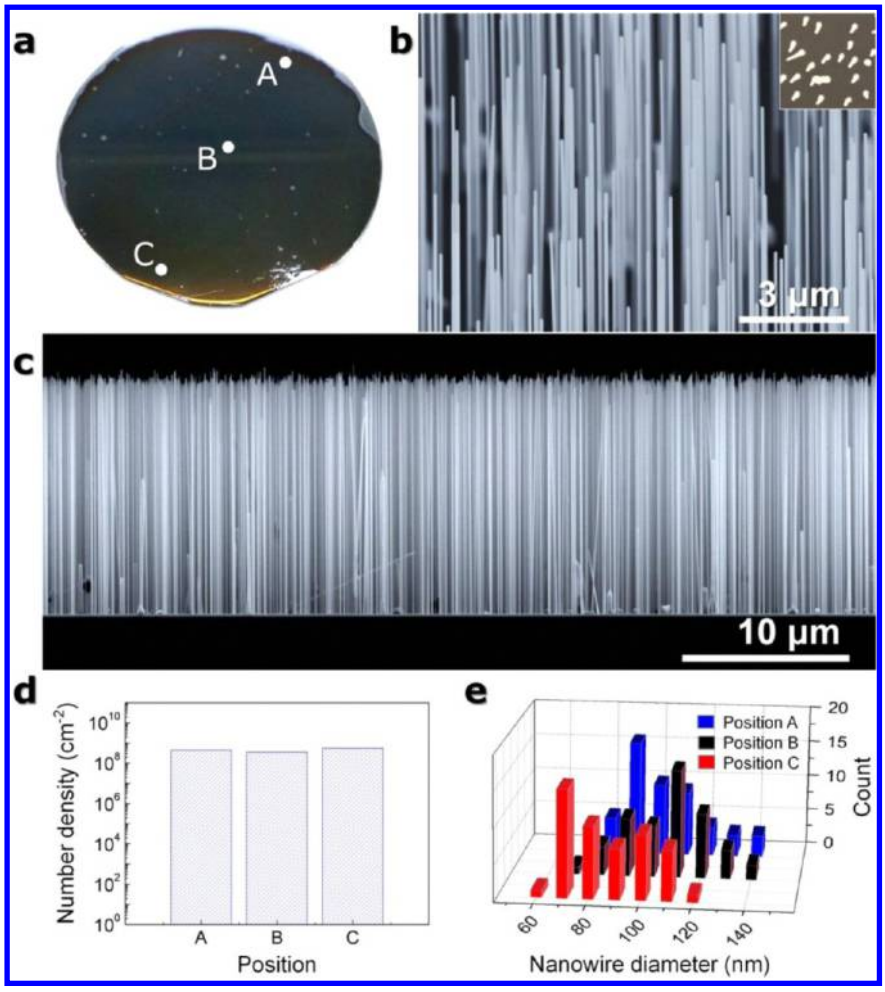

Figure 1. Optical and SEM images of the $InAs_yP_{1-y}$ nanowire array. (a) Optical image of the $InAs_yP_{1-y}$ (y = 0.75) nanowires grown on a 2 in. Si(111) wafer. (b) 45° tilted SEM image showing that the nanowires are vertically grown on the substrate. Inset is a top-view SEM image over an area of 4 μm^2, from which the number density of the nanowire array is estimated to be 5.5 × $10^8/cm^2$. (c) Side-view SEM image showing that the average height of the nanowire array is 14 μm. (d, e) Number density (d) and diameter distribution (e) of the nanowire array at three different positions marked in a, demonstrating the high uniformity. Number density in d is on a log scale.

However, the nanowire geometry (*i.e.*, diameter, height, and density) varies significantly across the wafer. Furthermore, phase segregation of group III [*i.e.*, indium (In) and Ga] occurs in the nanowire and thus results in a curved shape and a broad photoluminescence (PL) spectrum due to the inhomogeneous strain and large composition distribution, respectively.[26]

In this article, we report the heteroepitaxial growth of ternary $InAs_yP_{1-y}$ nanowire arrays on Si using metal−organic chemical vapor deposition (MOCVD). The nanowires are uniformly grown across entire 2-in. Si(111) substrates, and their aspect ratios exceed 100 without the use of metal catalysts or pattern assistance. X-ray diffraction and PL spectra of the $InAs_yP_{1-y}$ nanowire arrays exhibit a very narrow full-width at half-maximum (fwhm), indicating strong homogeneity of both individual NWs, as well as the NW array, across the entire wafer. Heterojunction solar cells composed of n-type $InAs_yP_{1-y}$ and p-type Si are fabricated and measured. The conversion efficiency of the heterojunction solar cells further increases *via in situ* growth of n^+-InP shells. These ternary III−V semiconductor nanowires on Si have potential applications for a diverse array of semiconductor devices, such as monolithic tandem solar cells,[27,28] high-performance transistors,[1] quantum information devices,[29] and light-emitting diodes.[6]

RESULTS AND DISCUSSION

An optical image of the $InAs_yP_{1-y}$ ($y \approx 0.75$) nanowire array grown on a 2 in. Si wafer is shown in Figure 1a. Fairly uniform diffraction color on the surface implies that the variations in height, diameter, and number density of the nanowires are small. Scanning electron microscope (SEM) images in Figure 1b and c show that the nanowires are grown vertically on the Si(111) substrate without any sign of bending. For the growth of the nanowires, an oxide-free Si wafer was dipped in poly-L-lysine (PLL) solution for 2 min and rinsed. Then, the Si wafer was promptly loaded into the MOCVD reactor. After the temperature was stabilized

at 610 °C under H_2 ambience, AsH_3 first flowed into the reactor for 1 min, and then PH_3 and TMIn were added for the nanowire growth. The detailed growth procedure can be found in the Experimental Procedures section. Self-assembled growth of In(Ga)As nanowires on Si has been previously reported.[26,30,31] In a lattice-mismatched system (*e.g.*, InAs/Si), the strain energy at the heterointerface is usually relieved by means of isolated island formation.[32] In these islands, crystallization occurs mostly in the ⟨111⟩ direction,[33] because lateral growth is not energetically favorable since the interface is elastic. As is known, the condition to form islands without a wetting layer (Volmer−Weber mode) in heteroepitaxy can be expressed by $\gamma_s < \gamma_i + \gamma_a$, where γ_s, γ_i, and γ_a are substrate surface energy, interface energy, and adlayer surface energy, respectively.[32] This indicates that an increase of interface energy γ_i due to increased lattice mismatch can promote the formation of islands, thus facilitating growth of nanowires; however if γ_i is too large, nucleation would be difficult. A short immersion in poly-L-lysine forms a thin polyelectrolyte layer on the Si wafers, resulting in a positively charged surface.[34] PLL solution has been used for the growth of Au-catalyzed nanowires because the positively charged surface attracts negatively charged Au and prevents the Au nanoparticles from clumping.[9,35] Similarly, we believe that the electrostatic interaction between the positively charged Si surface and negatively charged arsenic (As) should promote better adhesion and subsequent reaction with the Si surface. An attempt to flow TMIn prior to AsH_3 significantly decreases the number density and coverage of the nanowires, implying that positively charged In species inhibit nucleation. Crystal growth of InAs nanowires using self-assembled organic coating (*i.e.*, allyl alcohol) has been reported by the Samuelson group.[36] However, the organic-coated template in their case needed to be exposed in air for several hours. It was assumed that the complementary oxide pattern formed acted as a growth inhibition mask, while the organics were burned in growth to expose clean Si for selective area epitaxy.[36] In contrast, an increase of ambient exposure time after PLL treatment results in a decrease of number density and growth area of the nanowires in our case. Furthermore, the base diameter of the nanowire can be tuned from 30 to 300 nm with growth parameters, indicating the nanowire is not grown *via* organic-templated hole pattern. Note that PLL treatment could potentially cause contaminations during growth since it was reported that the presence of lysine was found on InP surfaces even after initial annealing at 600 °C although removed after prolonged annealing.[37] However, the morphological effect of PLL is certain. For comparison, InAs nanowires were grown on Si(111) substrates with and without PLL treatment (Figure S1 of the Supporting Information). Clearly, the uniformity, density, and growth area are dramatically improved with PLL treatment. Furthermore, ternary $InAs_yP_{1-y}$ nanowires do not grow at all on Si without PLL treatment. Figure 1d and e are the number density and diameter of the nanowires measured at three different positions on the PLL-treated wafer (*i.e.*, A, B, and C shown in Figure 1a). The nanowire density varies from $3.5 \times 10^8/cm^2$ to $5.5 \times 10^8/cm^2$ across the wafer. The average diameter of the nanowire array is 98 nm, and the variation of the diameter is ±40 nm. The average height of the nanowires is 14 μm for 40 min growth, and the variation is less than 2 μm over the entire Si wafer. These distribution statistics across an entire 2 in. wafer confirm wafer-scale uniformity of this growth method.

To understand the structural properties of the $InAs_yP_{1-y}$ (y = 0.75) nanowires, electron microscopy analyses have been performed (Figure 2). A high-resolution transmission electron microscopy (HR-TEM) image taken near the middle of the nanowire in height is shown in Figure 2a. The nanowire possesses a zinc-blende (ZB) crystal structure with a high density of stacking faults or twining along the growth direction, very similar to other demonstrations of nanowires grown *via* catalyst-free methods.[1,26,30] The existence of stacking faults is also supported by the presence of streaks along the ⟨111⟩ direction of the selected area electron diffraction (SAED) pattern shown in Figure 2d (A).[38] Shown in Figure 2b is a high-angle annular dark-field (HAADF) scanning (S)TEM image, which is highly sensitive to variations in the atomic number of the atoms. Remarkably, phase separation of ternary elements, which is occasionally shown in ternary nanowires grown on Si,[26,39] is not observed. Note that the increase of contrast toward the center of the nanowire is attributed to thickness contrast. Shown in Figure 2c is a cross-sectional TEM image taken at the interface between Si and $InAs_yP_{1-y}$. The heterojunction is atomically abrupt and free from antiphase domains or threading dislocations even though the existence of sporadic misfit dislocations is observed, as indicated by arrows. Shown in Figure 2d (B), (C), and (D) are SAED patterns that are taken at the positions marked by (B), (C), and (D) in Figure 2c, respectively. Spot splitting shown in Figure 2d (C) is evidence of diffraction from both Si and $InAs_yP_{1-y}$ planes at the heterointerface. Moreover, clear spots of SAED patterns without a streaky line indicate that the $InAs_yP_{1-y}$ nanowire is single-crystal ZB crystal structure, and more importantly, no stacking faults or twin defects are observed near the heterojunction.[1,19,33] This indicates that the stacking faults in the crystal arise after island formation on Si, implying that an optimized growth condition may allow the formation of single-crystal ZB structure along the entire nanowire length. The twinning in Figure 2a appears to be almost periodic, which is observed in many parts of the nanowire. This may be an indication of a cyclic crystal assembly regime and further supports the supposition that stacking-fault-free growth can be achieved under certain growth

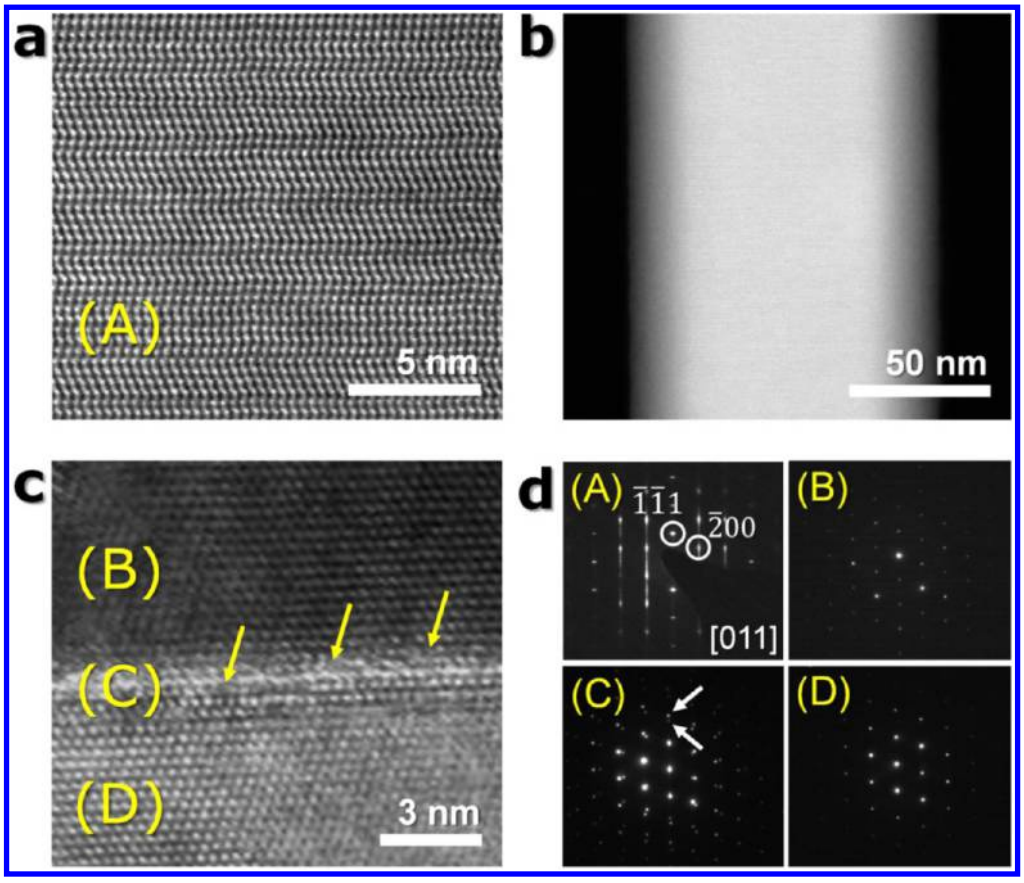

Figure 2. Electron microscopy characterization of $InAs_yP_{1-y}$ nanowire. (a) HR-TEM image taken near the middle of the nanowire in height shows massive stacking faults along the growth direction. (b) HAADF-STEM image of the nanowire presents uniform distribution of ternary elements. (c) Cross-sectional TEM image taken at the epitaxial interface of $InAs_yP_{1-y}$ (bottom) and Si (top). Sporadic dislocations are indicated by arrows. (d) SAED patterns recorded at four different positions marked in a (A) and c (B−D).

conditions. Cross-sectional TEM images and SAED patterns have been taken at several more places, confirming that the nanowire forms a single-crystal structure near the heterointerface (Figure S2 of the Supporting Information).

Tuning alloy composition of the ternary nanowires is imperative for a number of potential applications. Shown in Figure 3a is the PL spectrum measured at 77 K for the $InAs_yP_{1-y}$ nanowire array with and without an *in situ* grown InP shell. The peak position is located at 0.62 eV, corresponding to an As composition (y) of 0.75, based on the equation given by Antypas and Yep[40] as $E_g = 1.416 - 1.276y + 0.281y^2$. Importantly, the fwhm of the PL peak is 51 meV, which is comparable to that of the narrowest peaks reported for ternary III−V nanowires grown *via* the SAE method.[41] The InP passivation layer has a higher band-gap energy than the $InAs_yP_{1-y}$ core and can reduce surface recombination. Without the InP passivation, the PL signal was ~50 times weaker. The importance of passivation for device applications will be discussed later. The alloy composition of the $InAs_yP_{1-y}$ nanowires is further examined by the HR-XRD spectrum, as seen in Figure 3b. A Si(111) substrate peak is located at 28.4° in 2 theta scale, and the peak at 25.6° corresponds to the ZB form of $InAs_{0.75}P_{0.25}$, which is deduced from the lattice constants of InAs and InP using Vegard's law. To investigate the compositional gradient, EDX has been performed along the nanowire length, as shown in Figure 3c. The As composition, y, calculated from atomic counts of EDX is 0.74 ± 0.04 over the entire nanowire length. Importantly, no significant variation of the alloy composition is observed along the nanowire height. We do not expect much composition variation in the radial direction either, although no radial EXA analysis was performed. This is because the self-assembled growth in this work occurs only *via* the vapor−solid (VS) growth mode,[33] in contrast to the metal-catalyzed vertical nanowires, where alloy composition could exhibit a distribution[42] due to the coexistence of VLS and VS growth modes.[17,42] The arrow XRD and PL peaks further support that the nanowires have uniform alloy composition across the nanowires. In addition, the absence of bending in the nanowire morphology as seen in the inset of Figure 3c indirectly confirms that the alloy composition is uniformly distributed across the nanowire. Otherwise, uneven strain is applied along the nanowire, resulting in a

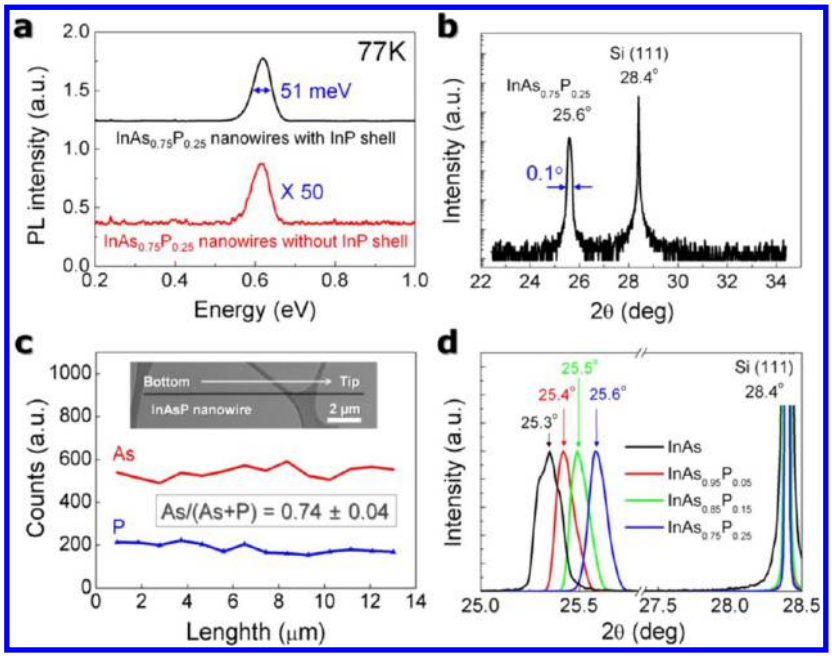

Figure 3. Characteristics of alloy composition of the $InAs_yP_{1-y}$ nanowires. (a) Low-temperature PL spectra of the $InAs_{0.75}P_{0.25}$ nanowire array before and after InP passivation. (b) XRD spectrum of the $InAs_{0.75}P_{0.25}$ nanowires on the Si(111) substrate. The peak from $InAs_{0.75}P_{0.25}$ is located at 25.6° along with the substrate peak to the right on a log intensity scale. (c) EDX line profiles of the $InAs_{0.75}P_{0.25}$ nanowire. Inset is the TEM image of the nanowire, showing the points where EDX is performed. Calculated As composition is 0.74, which is in good agreement with the PL and XRD results. (d) XRD spectra of the $InAs_yP_{1-y}$ nanowire array with different alloy compositions. Each XRD spectrum shows the Si(111) substrate peak at 28.4°, along with the epitaxial $InAs_yP_{1-y}$ peak to the left on a linear intensity scale.

curvature in shape.[26] Tuning alloy composition of the $InAs_yP_{1-y}$ can be achieved by changing the molar ratio of group V during growth, as seen in Figure 3d. The relationship between the alloy composition of the $InAs_yP_{1-y}$ in the solid state and the molar ratio of the gas phase group V precursors is shown in Table S1 of the Supporting Information. Although we report here a range of only $x = 1-0.75$ ($y = 0-0.25$) due to the limitations of the mass flow controllers on our MOCVD system, we believe a much wider range of uniform, structurally and compositionally homogeneous, and high-aspect-ratio $InAs_xP_y$ nanowires can be formed on Si.

Epitaxially grown III–V nanowires on Si have been fabricated into diverse electrical and optical devices such as light-emitting diodes,[6] field-effect transistors,[1,43] and high-sensitivity photodetectors.[7] Furthermore, heterojunctions can be applicable to the multijunction solar cells[27,28] or Esaki diodes.[45,52] To investigate the electrical properties of the epitaxial interface, heterojunction solar cells composed of n-type $InAs_yP_{1-y}$ nanowires and p-type Si have been fabricated as seen in Figure 4a. Note that there is no parasitic film grown between the nanowires inherent to the growth mechanism;[30] thus p/n junctions form only between the nanowires and Si substrate. The dark $I-V$ curve (Figure 4b) is measured at room temperature, and the current density (J) is plotted on log scale. The rectifying ratio and ideality factor calculated from $I-V$ measurements are compared to those of the heterojunction (*i.e.*, III–V nanowire on Si), the homojunction (*i.e.*, III–V nanowires on III–V substrates, Si nanowires on Si substrates), and 2-D heterojunctions of III–V and Si formed *via* wafer bonding techniques, as seen in Figure 4c. A large rectification ratio of $\sim 10^3$ at ± 0.5 V and a low reverse leakage current density (*e.g.*, 2×10^{-6} mA/cm^2 at -0.5 V) imply that the heterojunction is type II, in which the conduction and valence bands of the p-Si are higher than those of n-$InAs_{0.75}P_{0.25}$.[51] Even though the rectifying ratio of the diode varies with the amount of doping, a relatively large rectifying ratio is achieved compared to those of nanowire-based diodes. More importantly, the ideality factor extracted from a linear portion of the $\ln(J)-V$ plot is 1.4, which is better than those of the III–V on Si formed *via* the SAE method[19,44] or wafer bonding technique.[50,51] Remarkably, the ideality factor of our $InAs_yP_{1-y}$ nanowire on Si is comparable to those of the state-of-the-art homojunction nanowires.[47,48]

While surface recombination affects most semiconductor optoelectronic devices, nanowire-based devices are especially susceptible to surface recombination of photogenerated carriers due to their large surface-to-volume ratio.[53−56] Figure 5 shows energy band diagrams of the n-$InAs_yP_{1-y}$ core (a) and n-$InAs_yP_{1-y}$/n-InP core/shell (b) structures. In the core nanowire, there is a high density of surface states along the surface of $InAs_yP_{1-y}$, which act as efficient recombination centers for photoexcited electrons and holes, thus reducing the overall short-circuit current of the solar cells. In the $InAs_yP_{1-y}$/InP core/shell (b) structure, however, electron–hole recombination through surface states on the surface of InP is significantly reduced due to the spatial

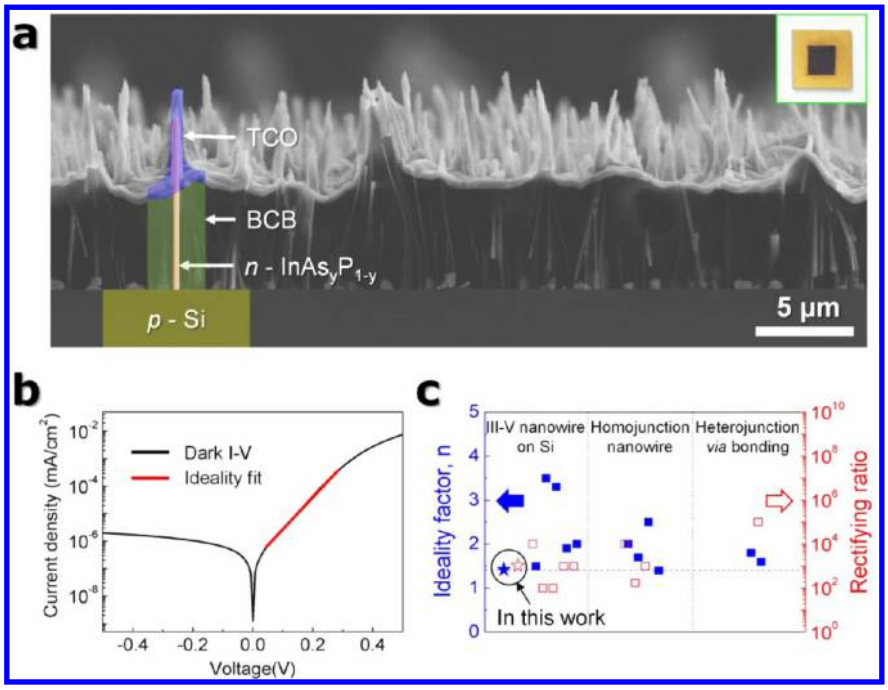

Figure 4. Electrical characterization of the heterojunction solar cells composed of an n-$InAs_{0.7}P_{0.3}$ nanowire array on a p-Si(111) substrate. (a) Cross-sectional SEM image of the solar cells showing that the tips of the nanowire array contact a TCO. Inset is an optical image of the fabricated device, showing the active area of 0.09 cm^2. (b) Dark *J*−*V* characteristics at room temperature. (c) Ideality factor and ratifying ratio compared to those of the diverse semiconductor junction (*i.e.*, III−V nanowires on Si, III−V nanowire on III−V, Si nanowire on Si, and III−V film on Si *via* wafer bonding technique).[26,30,43−51]

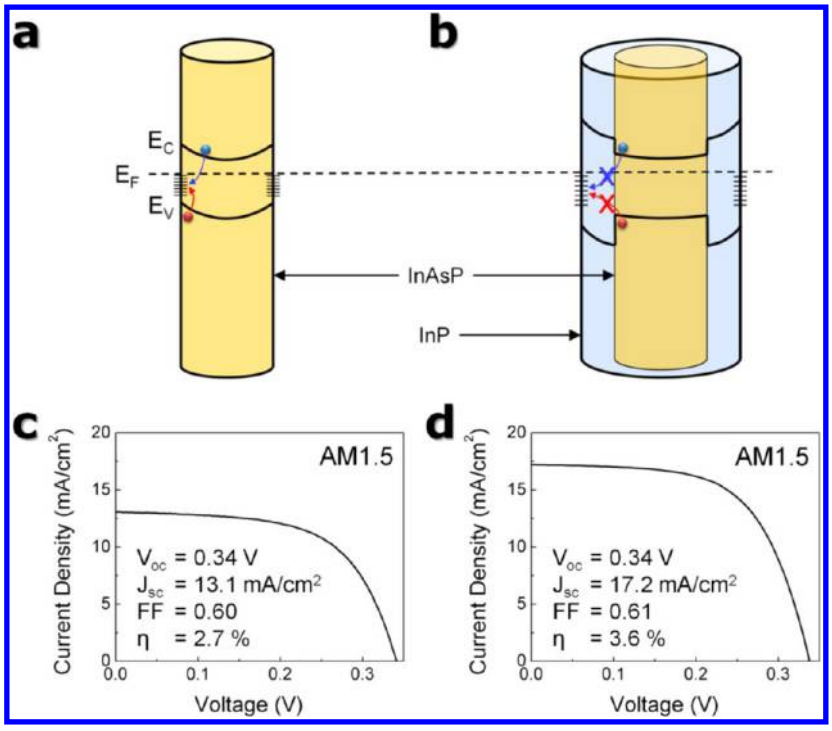

Figure 5. Characterization of the heterojunction solar cells. (a, b) Band diagram of the $InAs_yP_{1-y}$ nanowire without (a) and with (b) an InP shell. Defect states along the surface of the nanowire act as efficient recombination centers for photogenerated carriers. Core−shell structure can spatially separate the carriers from the surface, thus reducing surface recombination. (c, d) 1 sun *J*−*V* curve for the n-$InAs_{0.75}P_{0.25}$ nanowire/p-Si solar cells without (c) and with (d) an n^+-InP passivation layer.

separation between charge carriers and surface states, which increases short-circuit current. It is obvious that there is an optimal thickness of the InP shell layer when considering light absorption and surface passivation effects. In other words, a thicker shell might reduce electron−hole recombination, but the light absorption

within the shell layer cannot contribute to the solar cell current. We found that the optimal thickness of the shell layer was ~20 nm. Shown in Figure 5c,d are the *I*−*V* characteristics of the heterojunction solar cells under AM 1.5 (100 mW/cm^2) conditions at room temperature. The open-circuit voltage (V_{oc}), short-circuit current (J_{sc}), fill factor (FF), and energy-conversion efficiency (η) are 0.34 V, 13.1 mA/cm^2, 0.6, and 2.7%, respectively, for n-$InAs_{0.75}As_{0.25}$/p-Si and 0.34 V, 17.2 mA/cm^2, 0.61, and 3.6%, respectively, for the n$^+$-InP-passivated n-$InAs_{0.75}As_{0.25}$ nanowire/p-Si. The V_{oc} value of this heterojunction solar cell is slightly low based on the band-gap energy of the $InAs_{0.75}P_{0.25}$ nanowires. Misfit dislocations and band alignment at the heterojunction may result in a reduction of the V_{oc} value. Note that the J_{sc} increases more than 30% *via* InP passivation mainly due to the reduction of carrier recombination near the surface. The improvement in surface recombination can also be seen in our improved PL from the InP-passivated NWs. Thus, both our PL and solar cell characterization demonstrate that surface passivation is essential for the nanowire-based semiconductors because of their large surface-to-volume ratio.

CONCLUSIONS

In summary, we have demonstrated a novel method to epitaxially synthesize structurally and compositionally homogeneous and spatially uniform ternary $InAs_yP_{1-y}$ nanowires on Si at wafer-scale. The high quality of the nanowires is reflected in the remarkably narrow PL and X-ray peak width and extremely low ideality factor in the $InAs_yP_{1-y}$ nanowire/Si diode. The conversion efficiency of heterojunction solar cells composed of n-$InAs_yP_{1-y}$ nanowires and p-Si is significantly enhanced through *in situ* passivation with an n$^+$-InP nanowire shell, indicating the importance of surface passivation for the nanostructured semiconductor devices. Large-scale, heteroepitaxial growth of III−V nanowires on a Si substrate could lead to other high-performance and low-cost device applications on Si.

EXPERIMENTAL PROCEDURES

Metal−organic chemical vapor deposition (AIXTRON A200) was used for the growth of $InAs_yP_{1-y}$. The 2-inch Si(111) wafer was cleaned with buffered oxide etch (1 min) and deionized (DI) water (2 s). Then, the wafer was immediately dipped in poly-L-lysine solution (Sigma-Aldrich Inc.) for 3 min and then rinsed in DI water for 10 s. The Si substrate was then loaded into the MOCVD reactor without any delay. The reactor pressure was lowered to 50 mbar with 15 L/min of hydrogen gas flow. Then the reactor was heated to growth temperatures (570−630 °C) and stabilized for 10 min. Arsine (AsH_3) gas first ran into the reactor for 1 min; then trimethylindium (TMIn) and phosphine (PH_3) gas flowed into the reactor. The molar flow (mol/min) of TMIn and AsH_3 was 2×10^{-5} and 2.2×10^{-4}, respectively. To control the composition of the $InAs_yP_{1-y}$ nanowires, the molar flow of PH_3 was changed in the range from 4.5×10^{-3} to 8.4×10^{-2} mol/min. For the growth of the InP shell on the InAsP nanowire surface, the growth temperature was increased to 650 °C under mixed group V flows (AsH_3 and PH_3). After the temperature was stabilized, the AsH_3 flow was stopped and the TMIn run valve was opened, simultaneously. Disilane (Si_2H_6, 0.02% in H_2) was introduced to achieve n-type $InAs_{0.75}P_{0.25}$ nanowires (4×10^{-9} mol/min) and an n$^+$-InP shell layer (2×10^{-8} mol/min). These flows correspond to doping concentrations of mid-10^{17} and low-10^{18} cm^{-3} for planar InP film, respectively.

The morphologies of $InAs_yP_{1-y}$ nanowires were investigated by scanning electron microscopy (Hitachi-S4700). The Philips X'pert system (PANalytical Inc.) was used for the high-resolution XRD spectra. Structural properties of the nanowires were examined by TEM (Titan 80-300, FEI Inc.) Focused ion beam imaging was performed for the cross-sectional TEM images. The atomic counts along the nanowire heights were measured using EDX equipped in the TEM machine. The X-ray spot size for the EDX was ~0.1 nm. Photoluminescence was measured by amplitude modulation step-scan Fourier transform infrared (FTIR) spectroscopy on a Bruker V80 V system. Excitation was provided by a 980 nm diode laser with 100 mW power. The incident light was modulated by a beam chopper, and the emission from the sample was collected through a ZnSe window and collimated by a Ge lens, which blocked the exciting laser from entering the FTIR. The PL spectrum was detected by a HgCdTe (MCT) detector and then sent to a lock-in amplifier. The dc output of the lock-in amplifier was then returned to the FTIR. Step-scan modulation can improve the signal-to-noise ratio significantly since it removes all background noise by modulating the detector signal and the exciting source at the same frequency. The short-circuit current (I_{sc}) and open-circuit voltage (V_{oc}) of the solar cells were measured using an AM 1.5 solar simulator (100 mW/cm^2). Short-circuit current density (J_{sc}) and energy-conversion efficiency (η) values were calculated using the top planar area of the solar cell, excluding the metal contact area.

For solar cells, a p-type Si wafer (1−10 Ω-cm) was prepared and the boron was thermally diffused on the backside to form a p$^+$ contact. After growth of the $InAs_yP_{1-y}$ nanowire array, BCB (Cyclotene 3022-35, Dow Inc.) was spin-coated at 3000 rpm on the nanowire side; then the sample was annealed for 2 h at 300 °C. Because the nanowires are very long (>10 μm) and thin (~100 nm), small portions of the nanowires (<10%) are broken during the BCB-filling process. The Cyclotene was etched with CH_4/O_2 gases using a reactive ion etching system until the tips of theh nanowires were slightly exposed. ZnO (700 nm thick) was deposited on the side where the nanowire tips were exposed, followed by gold electrodes (Ti: 10 nm/Au: 200 nm) on top of the ZnO pad. Ti/Au (10 nm/200 nm) was then deposited on the Si surface for the back metal contact. The fabricated device can be seen in Figure 4.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Additional SEM and TEM images and molar flow rate of metal−organic sources. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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