InAs Planar Nanowire Gate-All-Around MOSFETs on GaAs Substrates by Selective Lateral Epitaxy

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***Abstract*— High indium content III–V materials are one of the most promising candidates for beyond Si CMOS technologies. We present InAs planar nanowire (NW) MOSFETs grown directly on a semi-insulating GaAs (100) substrate by the selective lateral epitaxy (SLE) method via the metal-seeded planar vapor-liquid-solid mechanism. Despite a ∼7% lattice mismatch, in-plane and self-aligned single-crystal InAs NWs are grown epitaxially on GaAs. Such heterogeneous SLE provides a potential solution for the integration of different channel materials on one substrate. Gate-all-around MOSFET devices are fabricated by releasing the NW channel from the substrate through a combination of digital etching and selective etching processes. The device with a NW width of 30 nm and gate length of 350 nm shows an I_{ON}/I_{OFF} ratio of 10^4 and a peak transconductance of 220 mS/mm at $V_{ds} = 0.5$ V.**

***Index Terms*— III-V MOSFETs, InAs, VLS growth, nanowire, selective lateral epitaxy.**

I. Introduction

III-V MATERIALS, especially InGaAs with high In-content (In%), are promising candidates for future low-power logic applications due to their excellent electron mobility [1]. State-of-the-art InGaAs channel MOSFETs are mostly based on InGaAs closely lattice-matched to InP substrates [2], or extremely thin-body InAs films [3]–[5]. For in-plane nanowire (NW) channels fabricated by etching a thin film layer, it is difficult to achieve a high In% due to the lattice mismatch with respect to a common growth substrate, such as GaAs or InP. The bottom-up self-assembled vapor-liquid-solid (VLS) method, which utilizes a metal particle (usually Au) to seed and direct the NW growth [6], [7] can grow high-quality NWs on highly lattice-mismatched substrates as nanostructures can accommodate more strain than standard thin films [8], [9]. This provides a promising solution for the formation of true 3D channels with high In%, and the heterogeneous integration of n-channel and p-channel materials, such as InAs and GaSb, on a single substrate. However, one complication of such a self-assembly method is that the NWs mostly grow out of the substrate surface in the <111> directions and, therefore, much more complicated fabrication processes are required than planar devices [10]. Furthermore, the vertical architecture inherently incurs more parasitic capacitance due to contact pad overlapping, which affects the speed performance [10]. while vertical NW transistors will continue to be developed and assessed by researchers, we have shown that VLS growth can take place in a planar fashion where the NWs grow laterally and are self-aligned along certain in-plane crystal directions [6], [7]. Therefore, we call this particular VLS method selective lateral epitaxy (SLE), where the selectivity is provided by the metal seed particles and the epitaxial relationship to the substrate ensures high crystal quality. The planar NWs are completely compatible with standard planar processing technology. Many types of devices, including MESFETs [11], HEMTs [12] and MOSFETs [13], and simple circuits [14] have been demonstrated to show good performance by homogenous SLE, namely, GaAs planar NWs on GaAs substrates.

In this letter, we demonstrate for the first time a heterogeneous-SLE InAs NW gate-all-around (GAA) MOSFET on GaAs (100). The devices are realized by releasing the NW channel from the substrate using a combination of digital and selective etching, while keeping the source and drain in plane. This work demonstrates the feasibility of InAs-based low power FETs and future heterogeneous device integration using SLE.

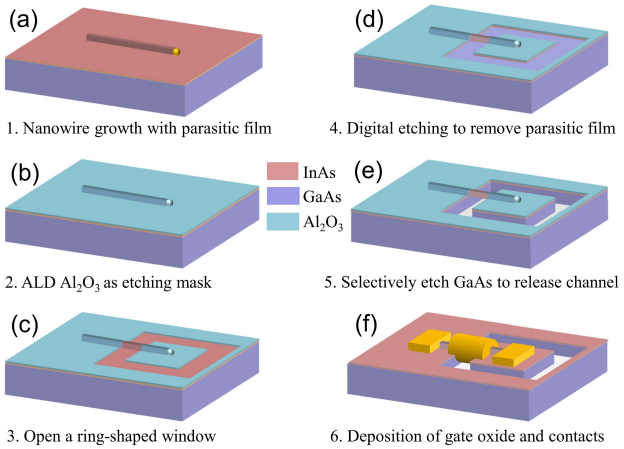

Fig. 1. Schematic diagram illustrating the key steps for the planar NW GAA MOSFET fabrication.

II. Experiments

Fig. 1 shows the process flow for the GAA MOSFET device fabrication, starting from planar InAs NWs directly

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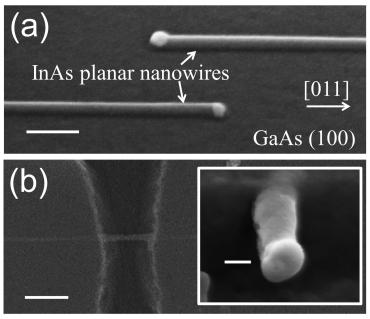

Fig. 2. (a) A 45° tilted SEM image of two as-grown InAs planar NWs on GaAs (100). Au dots are visible at the tips of the NWs. The scale bar is 100 nm. (b) SEM image showing a NW hanging over the trench after releasing (300 nm scale bar). The inset (50 nm scale bar) shows the cross section of a fabricated NW device with conformal gate metal coating.

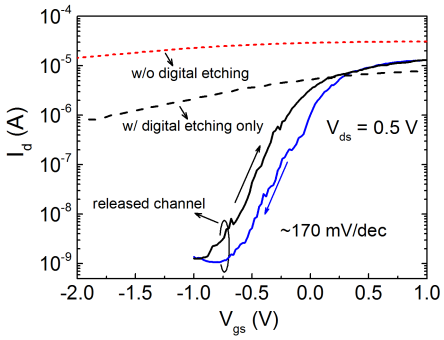

Fig. 3. Log-scale transfer characteristics of the InAs planar NW MOSFETs. Hysteresis could be due to the NW/oxide interface traps and/or mobile charges in the oxide.

grown on GaAs (100) semi-insulating (SI) substrates seeded by colloidal Au nanoparticles. The growth was carried out in a metalorganic chemical vapor deposition (MOCVD) system at 340 °C with trimethylindium (TMIn) and arsine (AsH_3) as precursors, without intentional doping. A typical growth rate was ~360 nm/min. A thin parasitic InAs film (with thickness on the order of a few nanometers) covering the entire sample surface was simultaneously formed during growth via the competing vapor-solid process, as illustrated in Fig. 1(a). The parasitic thin film, highly conductive according to the substrate current measurement, should be beneficial in reducing S/D resistance and can be readily removed in the channel region by digital etching [4], [5], as will be discussed later. Note that the parasitic thin film growth is much more sensitive to the growth temperature than the VLS NW growth; thus, can be reduced by lowering the temperature. Fig. 2(a) shows a SEM image of as-grown planar InAs NWs (width ~25 nm) self-aligned along either [011] or [0-1-1] direction, with Au seeds visible at the NW tips. We have found planar NWs grow along the projections of out-of-plane <111> directions on the substrate surface [11] (<111>B for GaAs planar NWs [11] and <111>A for InAs [7]). Therefore, unidirectional growth, which is desired for high-density device integration, can be achieved on a (110) substrate because there is only one out-of-plane <111>B or <111>A direction [11]. EDXS analysis has confirmed the NW to be InAs with no Ga detectable [7]. High-resolution TEM analysis can be found in [7], where the heterogeneous InAs planar NWs (with a Zincblende structure) are shown to be epitaxial to the GaAs substrate and free of stacking faults. NWs larger than 30 nm tend to form a zigzag trajectory on the substrate, presumably due to the strain effect.

To fabricate the MOSFET device, 12-nm Al_2O_3 was first deposited by ALD to be the etching mask for subsequent steps (Fig. 1(b)). A ring-shaped window was then opened on Al_2O_3 by e-beam lithography and BOE etching (Fig. 1(c)). In order to release the InAs NW from the underlying GaAs substrate, we removed the exposed InAs parasitic film (Fig. 1(d)) by digital etching [4], [5], where oxidation (at room temperature in a UV ozone cleaner from BioForce Nanoscience, Inc.) and oxide removal etching (by 1:1 HCl:H_2O solution) were performed alternately to etch III-Vs at ~1 nm per cycle. Two cycles of digital etching were sufficient for full removal of the parasitic film so that the underlying GaAs could be exposed. A trench was then formed on GaAs to release the center portion of the NW by selectively etching GaAs against InAs using NH_4OH:H_2O_2:H_2O (1:1:80) [15], similar to the release process of top-down InGaAs NW MOSFETs [2]. Fig. 2(b) shows a SEM image of a NW after releasing. 6-nm Al_2O_3 (EOT = 3 nm) was then deposited by ALD at 220 °C as the gate oxide, followed by the Ni/Au gate metal deposition by sputtering to provide conformal gate contact, as shown previously [16]. The inset SEM image of Fig. 2(b) shows the cross-section (after milling by focused ion beam (FIB)) of a fabricated device with the gate metal covering all around the NW. Finally, Ni/Au was evaporated for source and drain contacts after Al_2O_3 is removed on S/D region. No annealing was performed in the fabrication process. Although the current process leaves a large area of substrate covered by the parasitic film (Fig. 1(f)), which is undesired for circuit applications, in principle we can keep only the parasitic film in the S/D region by patterning.

III. Results and Discussions

Fig. 3 shows the log-scale transfer curves (V_{ds} = 0.5 V) of InAs NW MOSFETs with different fabrication schemes. The NW width, d, of these devices is ~30 nm. The device fabricated without digital etching and NW releasing (i.e., using as-grown NWs) showed very poor gate control (red, short-dashed curve). The as-grown substrate surface leakage current was measured to be 1-2 μA from two contacts not connected by a NW. This leakage path was removed by applying the digital etch treatment. The device with digital etching (applied to the entire substrate) showed some reduction of leakage current at $V_{gs} = -2$ V (black, long-dashed curve). Significant reduction of off-state leakage was observed only after releasing the NW channel. Shown in Fig. 3 by the solid curves, the I_{on}/I_{off} ratio is as high as 10^4 as V_{gs} varies from −1 V to 1 V, with the sub-threshold swing (SS) measured from the positive-sweep curve ($V_{gs} = -0.6$ V to −0.4 V) to be 170 mV/dec. This suggests the main leakage was induced by the bottom interface between InAs and GaAs. We speculate certain interface defects pin the

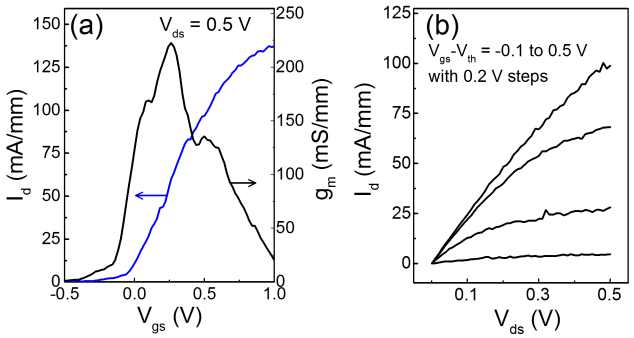

Fig. 4. (a) Transfer and transconductance curves of the GAA device with $d = 30$ nm an $L_g = 350$ nm. (b) Typical output curves of the device with the same dimensions. All numbers are normalized by πd.

Fermi level of InAs close to its conduction band so that the device could not be turned off completely. Note that we define the gate length, L_g, to be the trench width (350 nm in Fig. 2(b)), because the non-released gated portion cannot be well modulated. The DIBL of the devices is ~0.3 V/V. The on-state transfer curve and typical output characteristics of the GAA device are shown in Fig. 4. The threshold voltage is ~0 V. The device shows a peak extrinsic transconductance (g_m) of 220 mS/mm at $V_{ds} = 0.5$ V. The R_{on} is measured to be 4.1 Ω·mm at $V_{ov} = 0.5$ V. Both are normalized by πd.

The *SS* and g_m reported here are decent compared to other III-V NW devices summarized in [17], but are not as good as the state-of-the-art vertically grown VLS InAs NW device [18] and top-down InGaAs in-plane NW devices [2]. However, we note our device has a thick EOT (3 nm) and long L_g (350 nm) while both the state-of-the-art works above have an EOT of ~1 nm and a much shorter L_g. We estimate the interface trap density D_{it} from *SS* by $SS = (1+q\pi dD_{it}/C_{ox})\cdot 60$ mV/dec, where q is the electron charge and C_{ox} is the oxide capacitance per unit length. Thus, D_{it} is 1.6×10^{13} cm^{-2}eV^{-1}. We also extract the field-effect electron mobility, μ_{FE}, using the peak g_m measured at $V_{ds} = 0.05$ V. The gate capacitance was simulated by Nextnano [19] and estimated to be 1 pF/cm at the peak g_m. D_{it} (1.6×10^{13} cm^{-2}eV^{-1}) was added to simulate the C-V stretch-out. The μ_{FE} is estimated to be 2730 cm^2/V·s, which appears to be lower than those reported in [20]. We believe by scaling down L_g, EOT and contact resistance, the device performance can be further improved.

In summary, we have presented experimental results of InAs planar NW GAA MOSFETs grown by SLE on highly-mismatched GaAs substrates. Future studies will involve yield improvement and growth of planar p-channel (for example, GaSb) NWs. One way to integrate p- and n-channel NWs for CMOS is through multi-level planar VLS method, with the NWs from the first level of growth masked before patterning seed particles for the second level growth of a different material. Fabrication of lateral p-n heterostructures with only one level of seed particle patterning is also possible. In addition, we note that using Au seeds is not desired for integration with Si CMOS. VLS growth of InAs NWs by CMOS compatible metal seeds, such as Ni, has already been demonstrated [20]. SLE with a non-Au seed should be feasible and will be pursued in our future research.

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