Renee Tiger

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SUMMARY

Quality-focused **Electrical Engineer** with extensive experience in all aspects of front-end chip design. Specializes in VLSI/ASIC logic design, VHDL implementation, debugging through unit and chip simulation, meeting timing requirements and implementing on-chip test infrastructure. Recognized as an effective team player who utilizes excellent communication and problem-solving skills to consistently deliver quality, on-time designs.

TECHNICAL SKILLS

- VHDL
- Synthesis
- Boolean equivalency checking
- Unit simulation
- Verilog to VHDL conversion
- Script writing (Perl, TCL)
- Design for test (DFT)
- Top level chip integration
- Chip timing
- Chip simulation
- Initial hardware test
- Unix/AIX

PROFESSIONAL EXPERIENCE

Company, Rochester, NY **19XX – Current**

PCI Express Interface Logic Designer 20XX– Current

Designed various building blocks of the PCIE interface logic across multiple platforms on 5 I/O chips and 3 processors. Served on engineering team responsible for design, logic entry, verification and equivalency checking.

- Customized transmit half of PCIE interface for each chip, delivering high-quality, on-time logic.
- Delivered compile-clean design by taking ownership of clean-up of all logic in team's design.
- Added self-test, ABIST, LBIST, clocking, scan chains and startup testing to team's portion of the chip, ensuring seamless integration with the rest of this "pervasive" type logic.
- Converted the Verilog vendor-designed PCI cores to VHDL, meeting the requirement that it fit into the company architecture of each chip.
- Received 18 peer-given awards for working beyond job scope to accomplish team goals.
- Wrote scripts streamlining logic releases that made them consistent between all chips.

Chip Infrastructure Control Logic Designer 20XX – 20XX

Worked on team that designed test and maintenance infrastructure residing on every I/O chip in System z Mainframes. This includes scan chains, LBISTs, clocking, chip initialization, stopped clock testing and startup self-test.

- Customized logic to fit unique physical layout of each chip, making design functionally similar for every case.
- Communicated effectively to each team of chip designers what actions were needed, allowing for proper testing of chips for hardware defects in a real-world environment.
- Ran simulation of various tests, ensuring they could be run once wafers were built in the fab.
- Debugged issues with scan chain layout both in simulation and on the testfloor once hardware was available.

Company z10 I/O Sub-system Development Test Engineer 20XX – 20XX
Ran bringup testing on the I/O sub-system, with a focus on the 4 chips previously designed.

- Tested entire I/O subsystem of System z10 Mainframe, bringing it to market on schedule and in excellent working order.
- Designed and ran tests to check for functionality and reliability of system, as well as running tests that others requested to stress designs, ensuring customers received high-quality machines.

Self-Timed Interface Designer 20XX – 20XX
Designed proprietary interface to facilitate communication between I/O chips and memory on System z systems based on an architecture unique to Company. Worked directly on 6 chips and supported re-use of design on dozens more ending in 20XX.

- Wrote all logic of STI interface that resided on all I/O and memory chips, used for 15 years, and replaced by industry standard PCI-express.
- Designed STI as a building block, enabling it to easily be dropped onto any chip with no customization needed after being proven on the test floor and in the field.
- Developed close working relationship with simulation team, ensuring every aspect of design was functional and stable, including all error checking.
- Received award for extraordinary effort in completing a one-pass design on schedule.
- Recognized for excellence in high quality deliveries with the Systems Development Employee Excellence Award. Only 2 out of thousands of employees who excel in their responsibilities are selected annually.
- Continually introduced design innovations to improve the STI bus speed and minimize on-chip latency.

Cryptographic Processor Designer 1998 – 2001
Designed the DES cryptographic engine for a secure cryptographic card and an on-chip co-processor that worked directly with the System z processor.

- Designed an extremely high-speed DES engine to run highly secure encryption on System z mainframes designed for government and bank customers.
- Converted older designs from an IBM proprietary language (BDL/CS) into industry-standard VHDL.
- Led other designers to use VHDL by using original designs as teaching aid.

EDUCATION

BS, Electrical Engineering
Rochester Institute of Technology, Rochester, NY

PUBLICATIONS

- **"The Structure of chips and links comprising the Company Server z990 I/O subsystem," (2004),** ***Journal of Research and Development.*** Vol. 48, Number 3/4.
- **"Mars – A Candidate Cipher for AES," (1999).**