37th ANNUAL MICROELECTRONIC ENGINEERING CONFERENCE at RIT

April 16, 2019

Abstracts

Integration of hafnium oxide based ReRAM with CMOS for neuromorphic computing applications

Nathaniel C. Cady

Professor
Colleges of Nanoscale Science & Engineering
SUNY Polytechnic Institute

Neuromorphic computing systems can achieve learning and adaptation in both software and hardware. The human brain achieves these functions via modulation of synaptic connections between neurons. Memristors, which can be implemented as resistive random access memory (RRAM), are a novel form of non-volatile memory expected to replace a variety of current memory technologies and enabling the design of new circuit architectures. These devices are a prime candidate for so-called "synaptic devices" to be used in neuromorphic hardware implementations. A variety of challenges persist, however, for integrating memristors with CMOS, as well as for tuning device electrical performance. My research group has developed a fully CMOS-compatible integration strategy for RRAM-based memristors on a 300mm wafer platform, which can be implemented in both front end of the line (FEOL) and back end of the line (BEOL) configurations. With regard to memristor performance, we are focusing on strategies to reduce stochastic behavior during both binary and analog device switching. This is a key metric for neuromorphic applications, as variability in device conductance state directly influences the ultimate number of levels (weights) that can be implemented per synapse.

Bio:

Prof. Nathaniel Cady received his BA and PhD from Cornell University and has been a professor at SUNY Polytechnic Institute (in Albany, NY) sine 2006. His research spans the fields of biology and biosensors to nanoelectronics. His current work includes development of biosensors for Lyme disease diagnosis and nanoelectronics hardware for neuromorphic systems.

Fabrication of Photonic LPCVD Silicon-Nitride Waveguides

Robert Dalheim
RIT Integrated Photonics Group
Microelectronic Engineering
Rochester Institute of Technology

Abstract

The purpose of this project was to develop a repeatable process flow for the fabrication of Silicon-Nitride optical waveguides at RIT. Previous projects have fabricated optical waveguides out of amorphous silicon and polymers but never out of Nitride. The grating coupler pitch was varied from 700nm to 1500nm and the length was varied from 100µm to 1000µm. A target Nitride deposition thicknesses of 250nm, 500nm, and 750nm were deposited through LPCVD methods and were measured to be 150nm, 450nm, and 770nm. The thicknesses were chosen to be half the waveguide width for optimal transmission. Fabrication was successful for all three waveguide widths on the 450nm and 770nm thick Nitride wafers for both the Loopback and Ring Resonator designs as seen in figure 1. The grating couplers were able to resolve with pitches of 900nm to 1500nm but the 800nm pitch and under were overexposed and did not develop.

Optical testing was unable to be performed due to test setup being broken at the end of fabrication. Instead simulations of the test setup were done to see the optimal transmission for the 450nm thick and 1000nm wide Nitride grating coupler and waveguide. The test setup can vary wavelength from 1500nm to 1600nm so optimal transmission should have been about 1550nm. The best transmission results came from the tester head at an angle of 24 degrees and the grating coupler pitch of 1300nm showing a peak at the 1500nm wavelength.

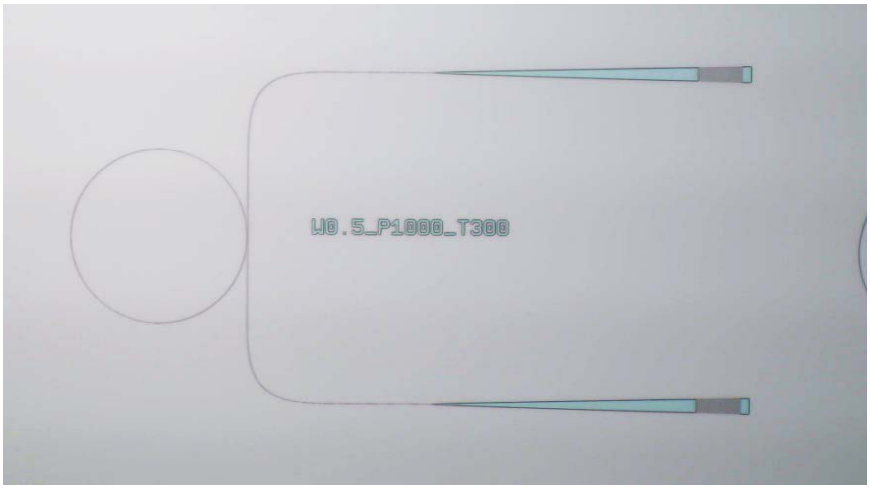


Figure 1. Microscope capture showing resolved Nitride ring resonator waveguide design with grating coupler pitch of 1000nm.

Biography

Robert Dalheim is a Microelectronic Engineering student from Brockport, New York. Robert has worked as a Validation and Test Engineer for Synaptics Inc. and as an Applications Engineer for On Semiconductor. He was unable to take a photonics-based course while enrolled at RIT but wanted to learn more about the industry. With the help and guidance of Dr. Preble and his graduate and PhD students, this project is the basis for further photonics research at RIT. Following graduation, Robert will be moving to Manassas, Virginia and working for Micron Technology as a Process Engineer.

Single Electron Transistors for Molecular Computer Readout

Matthew Filmer

Electrical Engineering, University of Notre Dame

As semiconductor manufacturers seek to reduce power dissipation it has become apparent that CMOS alternatives may be needed to enable the next generation of low-power microprocessors. A candidate technology is called “Molecular Quantum Dot Cellular Automata” (Molecular QCA), which stores binary state in the charge configuration of a pair of coupled mixed-valence molecules. Circuits can be constructed by assembling a network of QCA cells to allow Coulomb interactions between the cells. Readout of a computation requires determining the location of a single electron within a molecule. Single electron transistors as the most sensitive electrometers available can be used to make these measurements. As a step toward realizing a molecular computer my work focuses on developing and testing single electron electrometers for this application.

Fabrication of AlGaN/GaN High Electron Mobility Transistors

Vijay Gopal T.V.
Electrical and Microelectronic Engineering
Rochester Institute of Technology

Abstract:

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are of great interest for their high power and high frequency applications. HEMTs are already being used for a variety of applications that include power conversion, RF and microwave power amplifiers, as well as certain high temperature applications. This work presents the first attempt at RIT to fabricate AlGaN/GaN HEMTs. A fabrication process flow was designed, along with a mask set. The fabricated devices were tested electrically. Electrical results showed a minimal amount of gate control, but also a large amount of gate leakage. Electrical results also showed the presence of Schottky contacts within the source, drain, and gate regions. Based off of this first attempt, a baseline for future work has been established while also providing insight into future process improvements.

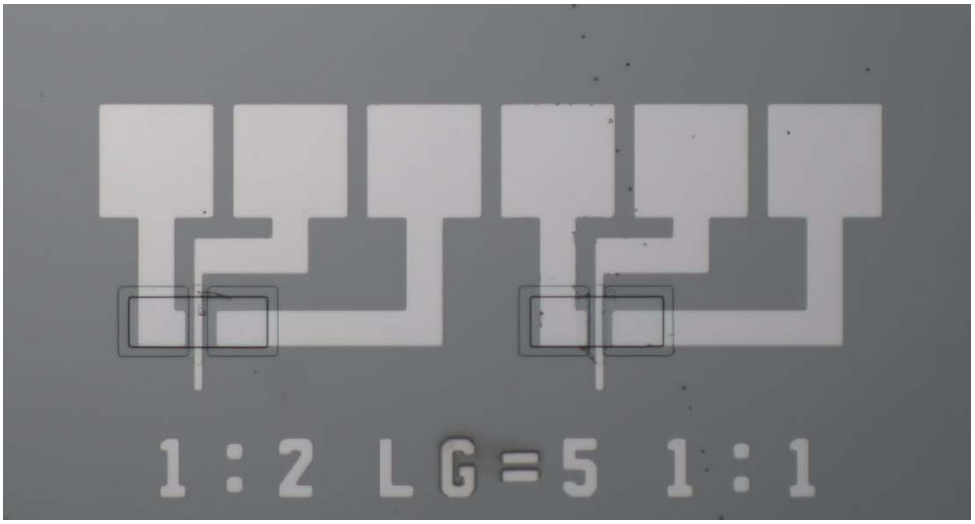


Figure 1:Microscope Image of Fabricated 5µm Devices

Biography:

Vijay Gopal is currently a senior pursuing his Bachelor's in Microelectronic Engineering. He has had three previous co-ops. His first was at the Stanford Nanofabrication Facility, second at Applied Image Inc., and third at Metrigraphics LLC. At Applied Image Inc., he worked as a Lithography Process Engineer and at Metrigraphics LLC, he worked as a Process Engineer. He is currently looking for employment as a Process Engineer within the semiconductor field.

Etching process characterization of Nitride layer and Poly silicon layer using TRION III Etcher

Sudmun Habib

Bachelor of Science in Microelectronic Engineering
Rochester Institute of Technology

Abstract:

As technology is evolving and we are pushing boundaries on how small and efficient our devices get, one of the main challenge that remains is for the technology that enables such process to develop evolves at the same rate. As we are reaching limits on our lithography process, etch recipes become vital and the need of direction anisotropic etch becomes critical. In this research the TRION III etcher will be characterized using all of its parameters (gas flow, power and pressure) to establish recipes for Nitride and polysilicon layer etch characteristics and profiles.

The key things to consider when doing Characterization of Etcher is to look into the layers Selectivity, etch rate and the profile. Over the lab process we were able to change process conditions and get data for etch rate and selectivity. It was seen the power and pressure becomes a key factor when it comes to etch uniformity and profile. O2 percentage plays a big part at the uniformity as it can be seen that without O2 etch Non uniformity drops to 19% which is highly undesirable. Micrograph imaging shows how nitride etch profiles looked good even at 1.0um imaging after the nitride and photoresist removal. Polysilicon etch result showed a huge change in etch rate compared to previous established data from the Drytek tool, the etch rate changed by 75 percent as we went from 300 seconds to 120 seconds of etch time. Furthermore profile testing using SEM imaging would allow us to establish how the selectivity and profile of the nitride and polysilicon layer to the underlying oxide layer looks like.

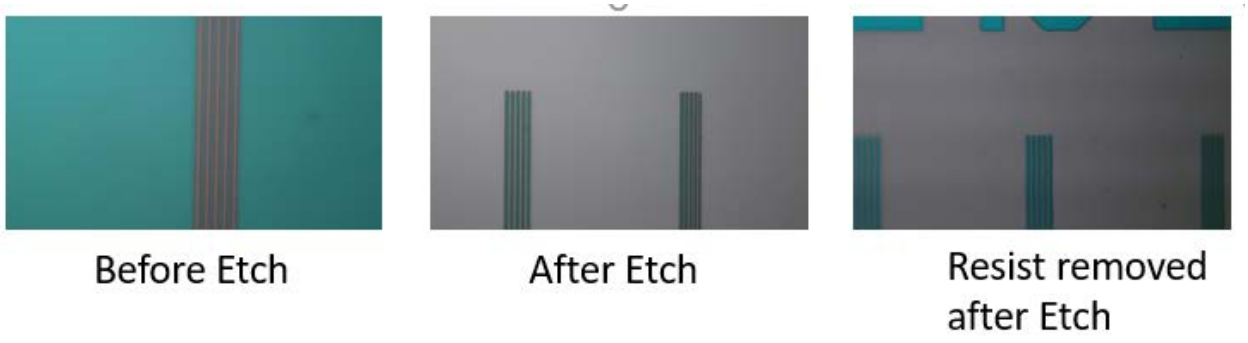


Figure 1. 1.0um line/space imaging before etch and after etch and after resist removal.

Biography:

I am a senior in the Bachelors of Science Microelectronic engineering program at RIT. I was born and raised in Bangladesh and completed my High School in 2014 Right after high school I joined RIT in 2014 August. Over the years through the Microelectronic engineering program I cooped at Rudolph Technologies Boston,MA. Through this I was able to co-write multiple papers along with the senior engineers on the topic of Lithography, Back end packaging, Coating of photoresist and photo die electrics. To name a few achievements – I was a recipient of bronze medal through the Duke Of Edinburgh program, Established my own Youth nonprofit organization to help my countries youth in achieving free education and getting proper nutrition.

Tape Transfer With 2-Dimensional Transitional Metal Dichalcogenides Materials

William Huang

Electrical and Microelectronic Engineering
Rochester Institute of Technology

Abstract:

This project is to expand RIT's knowledge on non-traditional 2D materials and to develop a tape-transfer process for single to double atomic layers of Molybdenum Disulfide from a substrate containing bulk MoS_2 to a blank substrate. The exfoliated materials will be inspected and characterized through both optical microscope and Raman Spectroscopy. The ultimate goal is to build it into devices to conduct electrical testing for its material and electrical properties. Material and electrical properties of the exfoliated materials will further be investigated and compared to MedeA simulation results. **Figure 1** demonstrates different characteristics measured in terms of Raman Shift dedicating to different atomic layering; bilayer, trilayer, bulk material from bottom to top. The tape transfer results were proved to be promising. Achieving for a bi-layer transfer is possible and a mono-layer exfoliation is also doable but with restriction on the inspection tool, a mono-layer transfer can only be assumed by visual inspection. Future work on the project will be to build a device with exfoliated monolayer materials and to conduct electrical testing for its material and electrical properties and confirm the simulation results.

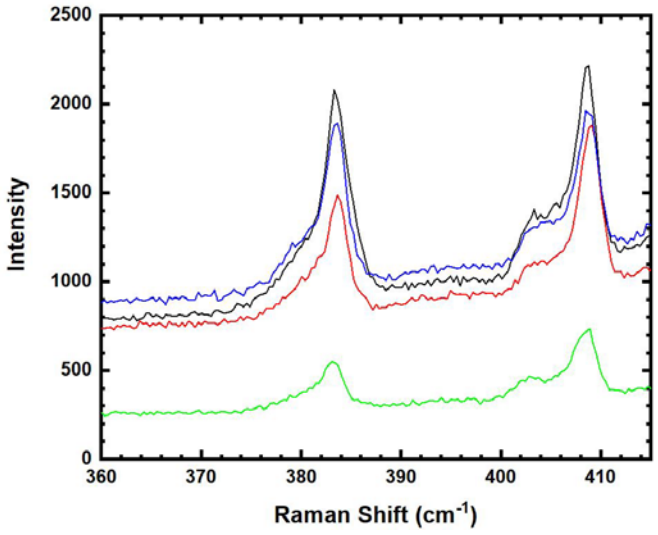


Figure 1. This figure demonstrates the different Raman Shift profile inspected on different atomic layers of exfoliated MoS_2

Biography:

William Huang, BS/MS Microelectronics Engineering and Materials Science and Engineering is from Taipei, Taiwan. Previously, he co-oped with Element Six Technologies, groups of de Beers company as a CVD Diamond Research Intern in Santa Clara California and AdarzaBio as an Engineering Intern in Rochester New York. He will be working under Dr. Puchades over the summer to conduct research into Carbon Nanotube Thin Film Transistors and return to campus next semester to continue some aspect of this project as well as to complete his master's degree in Materials Science and Engineering.

2D materials for a new generation of multi-functional devices

Steven J. Koester

Professor
Department of Electrical and Computer Engineering
University of Minnesota, MN 55455, USA

Two-dimensional (2D) materials are layered crystals, defined by strong intra-layer covalent bonds and weak inter-layer van der Waals coupling, that possess many unique and interesting properties. In this talk, I describe recent advancements on 2D materials, and discuss new device concepts in electronics, photonics, spintronics and sensing, with a focus on applications where these materials can provide improved performance or enable new functionality compared to conventional materials. Graphene is a 2D sheet of sp^2-bonded carbon atoms, and while it has limited usefulness for field-effect transistors, graphene has applications in a wide range of other fields. Graphene is an excellent sensor material due to its high surface sensitivity, and we have gone beyond conventional sensors and shown that this sensing capability can be transduced into the wireless domain by utilizing the quantum capacitance effect. More recently, we have shown that metal-oxide-graphene devices can be used to create atomically sharp "tweezers" for trapping biomolecules such as DNA at voltages as low as 700 mV, making them suitable for integration with CMOS readout circuits. We have also developed novel graphene-based spintronic devices, include devices for hard drive read heads and low-power spin- neuromorphic computing architectures. 2D semiconductors also have a multitude of uses as integrated electronic and photonic elements. In particular, we have shown that MoS_2, a transition metal dichalcogenide (TMD), is ideal for dynamic random access memories (DRAMs), where the wide band gap and heavy effective mass make it an ideal platform for ultra-low leakage access transistors. On the other hand, black phosphorus (BP), with its narrow band gap and low effective mass is ideal for use in high-speed photodetectors, high-performance MOSFETs and tunneling field-effect transistors.

Biography

Dr. Koester received his Ph.D. in 1995 from the University of California, Santa Barbara. From 1997 to 2010 he was a research staff member at the IBM T. J. Watson Research Center and performed research on a wide variety of electronic and optoelectronic devices, with an emphasis on those utilizing the Si/SiGe material system. Since 2010, he has been a Professor of Electrical & Computer Engineering at the University of Minnesota where his research focuses on novel electronic, photonic and sensing device concepts with an emphasis on 2D materials. Dr. Koester has authored or co-authored over 250 technical publications, conference presentations, and book chapters, and holds 68 United States patents. He is a Fellow of the IEEE.

Capping Layers for Increased Thermal Stability of IGZO Thin-Film Transistors

Jason Konowitch

Hirschman Research Group
Microelectronic Engineering
Rochester Institute of Technology

Abstract:

The goal of this project was to initially re-establish a baseline process for the fabrication of Indium-Gallium-Zinc Oxide thin-film transistors, shown in Figure 1, that have been a part of ongoing research here at RIT. After bringing the fabricated devices back into a reliable process, capping layer differences were to be investigated to determine their effects on device thermal stability. The time of the passivation layer anneal was varied between 3 and 4 hours for the primary lot and the temperature of the ALD capping layer was varied between 150°C and 200°C. The devices were tested and then thermally stressed on a hot plate for an hour at 140°C and 200°C. From the initial testing, it was shown that devices with 200°C ALD and with a 3 hour anneal had the best performance were the most thermally stable. After testing I-V characteristics, a length dependency was also found from the thermal stability in which the shorter devices remained operational after stress, whereas, longer devices became short circuits.

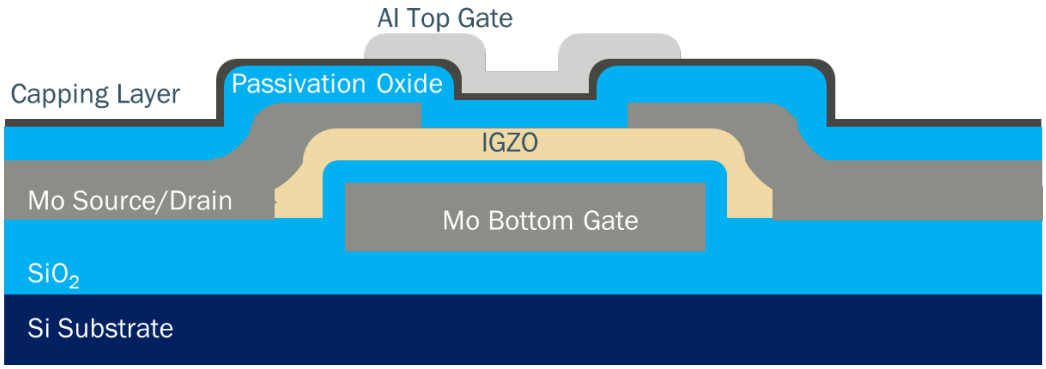


Figure 1. Cross section of an IGZO TFT.

Biography:

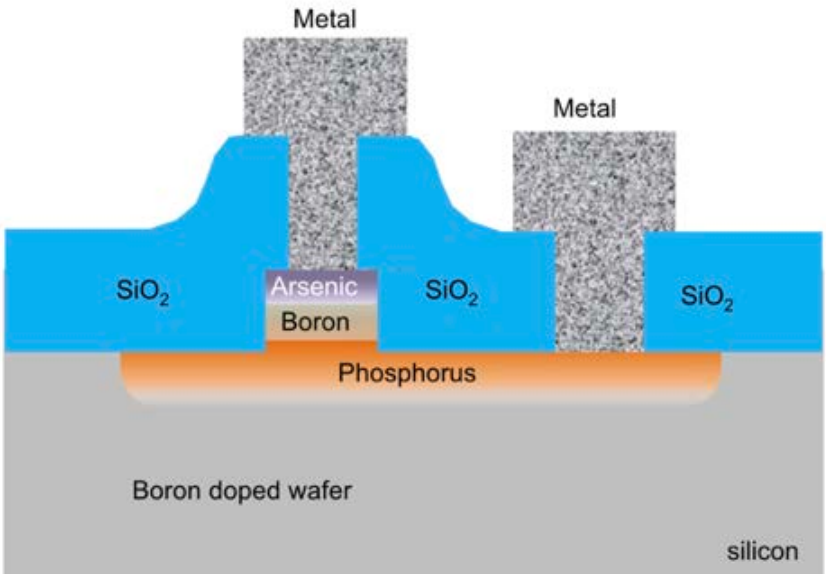
Jason Konowitch is from Richmond, Massachusetts and is a fifth year student in the BS/MS program for Microelectronics Engineering and Material Science. His senior project was chosen due to the fact that it overlaps his Bachelor's and Master's programs. He has had co-ops at Adarza Biosystems and here at RIT with Dr. Karl Hirschman's research group and has also worked as a math teacher at a Community College in Massachusetts. Following this semester he will remain at RIT to work on his thesis and graduate courses.

Biristor Array Investigation

Jeremiah Leit
Microelectronic Engineering R.I.T.

Abstract:

The biristor is a device that has interesting I-V characteristics. When it is current driven it is the reference device exhibits neural spiking. This neural spiking is characterized by a differing voltage at a steady current. The other method of operation is one in which a hysteresis loop is formed. This hysteresis loop can be used for hardware based encryption. This is because the device acts differently to the same stimulus based on previous results. The biristor that was fabricated at RIT was a vertical device modeled after the work of Dr. Jin Woo Han and Dr. Meyyapan however it did not appear to have either of these two operating modes and instead appeared to exhibit two stable resistance values. The devices that were fabricated at RIT were significantly larger by a factor of roughly 5 in the smallest case than those fabricated by Han and Meyyapan. The sweep from low to high results in high resistance while the sweep from high to low results in significantly lower resistance. This different result leads to the question of whether process variability or device size lead to a difference in I-V characteristics. Below is the structural cross-section of the device.



Biristor Cross-Section

Biography:

I am a fifth year student at RIT who is studying microelectronics. I have worked at the NPRL research laboratory working on III-V semiconductor solar cells. Another place where I have worked is the Femtosecond Laser Lab working on laser ablated materials as well as thermionic solar cells. Finally, I spent 6 months as a process engineering intern at Metrigraphics while there I worked on particle filters and optical encoders. I am a member of Phi Kappa Phi honor society and am graduating summa cum laude.

“Tiger Stripes” – A model for resolving complex process interactions in the pursuit of defect elimination

Chelsea Mackos

Director of Engineering, Solar Cells & CIC, SolAero Technologies

As the world leader in solar energy for space power application, SolAero produces more than 300 kilowatts of solar cells each year – in this context a high level of scrutiny is applied to yield loss, and in particular the fraction of that yield loss which is attributable to “Visual Defects.” This presentation will outline research and process development work completed to eliminate a Visual Defect in the solar cell’s anti-reflective coating (ARC), applied as a final step in solar cell processing to increase the light absorption of the cell. The team leveraged the distinctive “Tiger Stripe” pattern of the defect into novel experimentation wherein wafers were rotated in a unique orientation at each suspect-processing step in order to identify the point of initiation, and to eliminate multi-variate interactions that confounded the root cause of the defect. Careful observation of this wet processing step reveled the ultimate root cause
– a simple rinse operation caused residual chemical to dry on the wafer which when exposed to vacuum processing at ARC resulted in the unique visual characteristic of the defect of concern. While a straightforward adjustment to the parameters of the rinse eliminated the defect, the methodical and process driven approach to root cause identification used in this investigation continues to serve as a model at SolAero for de-convoluting complex process interactions in the pursuit of lower yield loss.

FeFET Fabrication and Characterization at RIT

Jordan Merkel

Electrical and Microelectronic Engineering Department
Rochester Institute of Technology

Abstract:

Hafnium oxide-based ferroelectrics are gaining popularity in the field of non-volatile memory due to their superior scalability in reference to traditional, lead-based ferroelectric materials and their compatibility with CMOS technology. Ferroelectric field-effect transistors (FeFETs) incorporate such materials in their gate stack, providing for bi-stable transfer characteristics and threshold voltages, which can be interpreted as storage values of 0 or 1. The difference between these threshold voltages is a FeFET figure of merit, referred to as the memory window (MW) of the device.

A process for fabricating n-channel FeFETs in-house at RIT has been developed, incorporating atomic layer deposition (ALD) of Al:HfO_2 and CMOS processing techniques. Test results of the first lot show signs of improper source/drain formation, evidenced in part by high off-state leakage and a poor on- to off-state current ratio; the root cause of improper formation is still being investigated. Nevertheless, ferroelectric behavior has been observed. Figure 1 shows the transfer characteristics of a representative FeFET from the first lot with a memory window of approximately 150mV. This result is comparable to that obtained from a device with a similar ferroelectric film in literature. The impact of threshold adjustment implantation on the transfer characteristics and memory window of the devices was also investigated, and ultimately found to shift both transfer curves of a given device without degrading memory window. To revive the current devices, monolayer doping (MLD) techniques will be employed to recreate source and drain regions, and devices will be retested; a new device lot will follow.

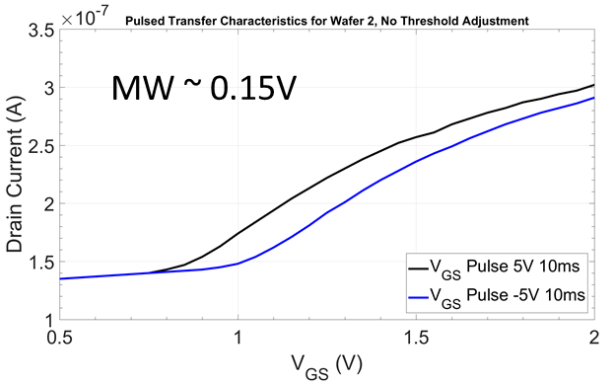


Figure 1. Transfer Characteristics of an n-channel FeFET shows Memory Window of 150mV.

Biography:

Jordan Merkel will be receiving a B.S. in Microelectronic Engineering from Rochester Institute of Technology in May of 2019. In August of 2019, he will be returning to work full-time at the Applied Technologies Laboratory for Northrop Grumman Corporation, where he has previously worked as a co-op student. Jordan has held two additional co-op positions at RIT in the microelectronic engineering department, assisting in research efforts pertaining to thin-film transistors, monolayer doping techniques and ferroelectric materials. He was recently named the 2019 Turkman Scholar and one of RIT's outstanding undergraduate students in 2018.

LivAbility Lab: Force and Position Monitoring System -MSD I

Nick Petreikis

Microelectronic Engineering
Rochester Institute of Technology

The goal of the LivAbility Lab project is to create a force and position monitoring system which can be used to evaluate the feasibility of assistive devices for individuals with movement impairments. To achieve this, resistive force sensors, beacon sensor tags, and accelerometers will be integrated into a system worn by the patient. Figure 1 shows a possible attachment option for the system. Safety of the user is vital to the success of the project. The system must not cause any impedance to the patient's ability to move. To be successful, the goal of the first semester is to complete the detailed design for the system and order all components. The goal of the second semester is to integrate all components into a robust system which is safe, accurate, and precise.

Figure 1. Possible attachment option for the system.

Nick Petreikis is a Microelectronic Engineering major graduating December 2019. He has done co-ops with ON Semiconductor and Texas Instruments. Nick is currently enrolled in Multidisciplinary Senior Design 1. At this time Nick does not have a full-time placement following graduation.

Demonstration of Record-High mm-Wave Power Performance using N-Polar Gallium Nitride HEMTs

Brian Romanczyk

Electrical and Computer Engineering Department
University of California Santa Barbara

Gallium Nitride high electron mobility transistors (GaN HEMTs) are proven to be well suited devices for highly efficient solid-state radio frequency power amplification, especially when high output power is desired. Existing GaN transistor technologies using the Ga-polar crystal orientation (0001) have been demonstrated operating at millimeter-wave frequencies (30 to 300 GHz). While these Ga-polar devices have demonstrated good large signal functionality, their performance has largely saturated. With growing interest in communication and imaging applications operating at mm-wave frequencies there is a need for transistors technologies with higher performance at these frequencies. This work focuses on the development and demonstration of mm-wave N-polar GaN HEMTs using a deep recess device structure. The internal polarization electric fields that are characteristic of c-plane GaN are inverted in the N-polar GaN orientation (000-1) relative to the Ga-polar orientation. This enables the deep recess device structure used in this work where a GaN cap layer is added into the access regions of the device. This GaN cap mitigates the impact of DC-to-RF dispersion and improves the conductivity of the access regions leading to the demonstration record-high output power density and power-added efficiency at operating frequencies ranging from 30 to 94 GHz. At 94 GHz, an unprecedented 8 W/mm of output power density with an associated 26.9% power-added efficiency has been obtained.

Super activation obtained by melt UV laser annealing of highly surface-segregated dopants in high Ge content SiGe

Leonard M. Rubin

Chief Device Scientist
Axcelis Technologies

Activation of surface segregated dopants above the solid solubility limit in a high Ge content SiGe substrate has been demonstrated by nanosecond melt UV laser anneal. This exceeds the activation possible with conventional solid-phase annealing. Segregation effects, strongly amplified by the phase changing of the partial melting of the sample during the annealing, play a key role explaining dopant profile redistribution and activation in Si-Ge alloys.

The RIT impact

Ken Way

Head of WW Business Development and Sales
Xilinx

The RIT Microelectronic Program is world renowned for effectively preparing students to enter the semiconductor world as productive process engineers. Nearly twenty five years ago, I was lucky enough to final place with Motorola Semiconductor landing a spot on their highly coveted Engineering Rotation Program in Arizona. On the first stop of a 12-month rotation, I spent the first 3 months of my post graduate career as a Yield Enhancement Engineer in the Motorola MOS 12 Fab where I made some important findings that allowed me the privilege to present at semiconductor conference and publish a paper, a fabulous start to my career in the fab. I was then given the rare chance to spend the next 3 months in the Digital and Analog Group as a Product Marketing Engineer where I spent time creating strategies, pricing and product plans, supporting sales and working with customers. I was forever hooked, engaging with business side was very exciting for me. Over the next 24 years, I played a significant role with some of the largest deals in the industry, enjoying the feeling of victory and the awful pain of defeat. I have played roles in IPO's, LBO's, acquisitions, valuations rising and falling, and today the dawn of Artificial Intelligence where my current company has developed a game changing 7nm device capable of driving the Adaptive intelligent world. My undergraduate experience at RIT helped create a solid foundation and was a key contributor to my ability to navigate through all of these experiences. Since a successful sales process relies heavily on trust and perceived competence, my success really took off when I effectively demonstrated and leveraged the knowledge I had about the design and fabrication of IC's coupled with the RIT brand name behind it further powering my credibility.

Biography: Ken leads the Xilinx data center business development and sales team responsible for the new "Alveo" product line of accelerator cards targeting the changing workloads of the modern data center. Ken is a sales executive leader with 25 years' experience in the semiconductor and systems industries with a proven track record of winning new business worth over $4B of lifetime revenue. Ken has successfully built and managed large-scale, global, direct sales/applications organizations, and channels that have consistently returned double digit revenue and market share growth. Ken and his teams have won the most coveted business in the industry and have been recognized by Tier1 customers and partners as "Supplier of the Year" and "Sales Team of the Year". Ken has developed a specialized skillset focused on the high growth Data Center, Cloud, Security and Telecom market segments targeting network and security manufacturers, cloud and data center operators, Fortune-5000 enterprise IT organizations, government networks and consumer product developers. Ken's executive sales management experience in the systems and semiconductor industries includes software, hardware, services and tools. Ken earned a degree in Microelectronic Engineering from the Rochester Institute of Technology, and has held senior sales leadership positions with Motorola Semiconductor, Freescale Semiconductor, Cavium, Tilera, Netronome and most recently as President and Chief Sales Officer with Napatech.

Fabrication of Sub-300nm Fins at RIT by Self-Aligned Double Patterning

Kelly Weiskittel

Electrical and Microelectronic Engineering
Rochester Institute of Technology

Abstract:

The goal of fabricating sub-300nm fins with the implementation of self-aligned double patterning (SADP) at Rochester Institute of Technology's (RIT's) Semiconductor & Microsystems Fabrication Laboratory (SFML) was not realized completely. A focus exposure matrix (FEM) was completed in order to qualify a new resist being used with the fabrication process that Christopher O'Connell developed for his graduate thesis. Manual spin coating of Spin-on-Carbon (SOC), bottom antireflective coating (BARC), and photoresist were all qualified with standard deviations in film uniformity of 1.56%, 0.47%, and 1.27%, respectively. A 2:1 ratio of AZ MiR 701 photoresist to PGMEA was used to thin the resist for implementation of a 300nm coat. Low pressure chemical vapor deposition (LPCVD) of silicon nitride as a spacer material was qualified with a ~64 Å/s deposition rate, a standard deviation in film uniformity of 1.49%, and a film etch rate of ~3 Å/s. Oxide deposition by in Applied Materials' P5000 TEOS chamber was qualified with an ~88 Å/s deposition rate and a ~32 Å/s etch rate in the reactive ion etch (RIE) etch chamber of the same P5000 tool cluster. In the RIE chamber, an etch rate of ~8 Å/s was qualified for the BARC layer. Upon etching of the oxide mandrels (Figure 1), angled sidewalls were observed. The absence of any hard mask on top of the oxide mandrel layer is likely responsibly for the lack of an anisotropic etch of the mandrel. The angled sidewalls prevented nitride spacers from properly forming around the mandrels.

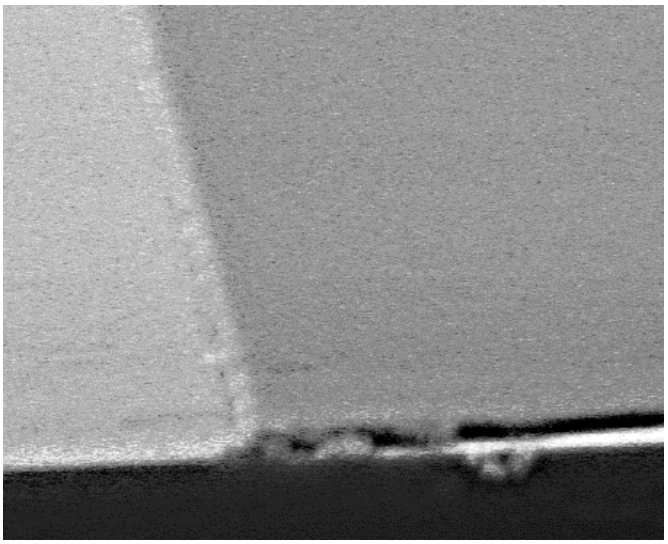


Figure 1. Zoomed-in image of wide oxide mandrel's sloped sidewall.

Biography:

Kelly Weiskittel is a fifth-year undergraduate Microelectronic Engineering student at Rochester Institute of Technology. Her advisor for this Senior Design project is Dr. Dale Ewbank. Previously she has completed cooperative education experiences with Welch Allyn as a test engineering intern and with Renesas Electronics as a photolithography process engineering intern. She will return to Renesas Electronics this summer of 2019 for full-time employment as a process engineer. Outside of her schooling, she is involved in RIT's Varsity Cross Country team, as a member from 2014-2017 and as a co-captain in 2018.

38th AMEC on April 13 and 14, 2020