Recreating History

Making the Chip that went on the Moon in 1969 on Apollo 11

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CREATIVITY + INNOVATION FESTIVAL

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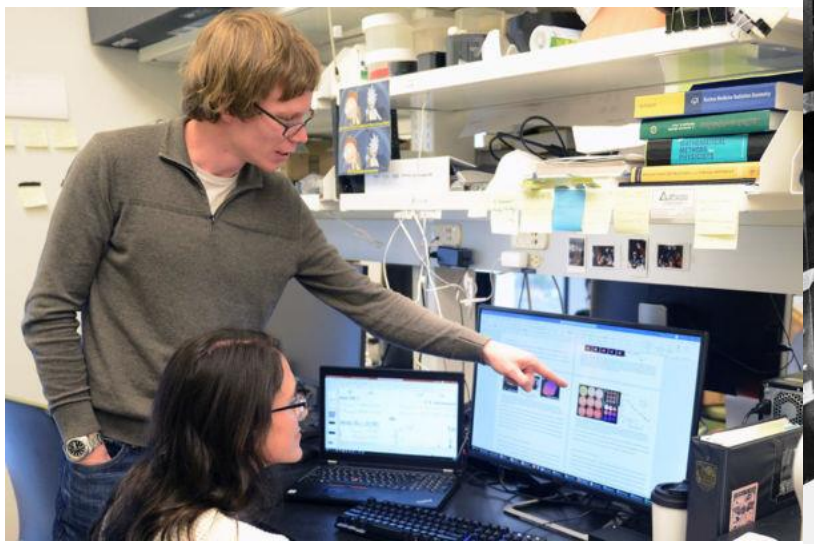
External Team Contributors

Jimmie Wayne Loocke; Ex NASA Technician, Founder of Space Computer.Org

Petr Bruza, Assistant Professor of Engineering, Dartmoth Engineering, Thayer School, Hanover, NH

Eldon Hall, Original AGC Designer

Jimmie Wayne Loocke



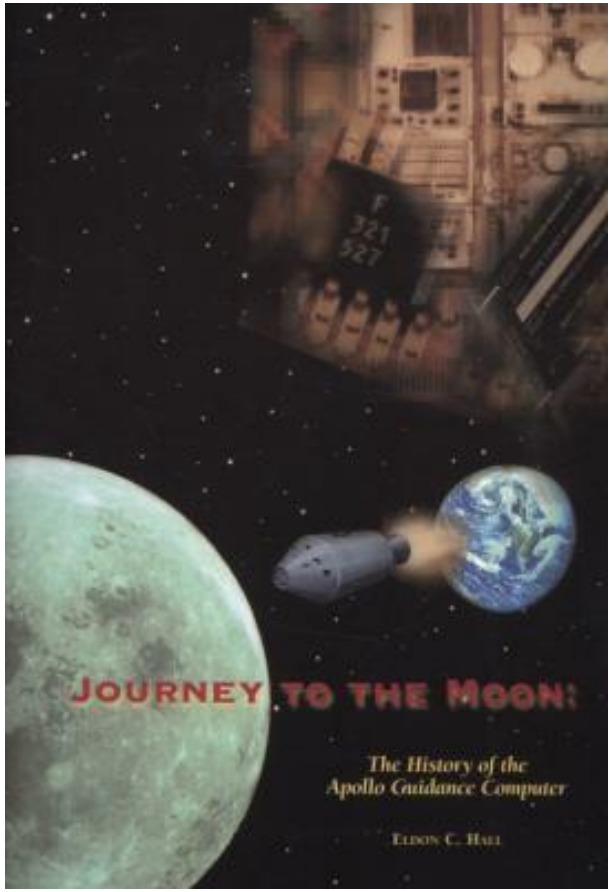
Petr Bruza

Eldon Hall inspects an AGC display and keyboard (DSKY). Photo: Charles Stark Draper Laboratory Archives

Eldon Hall

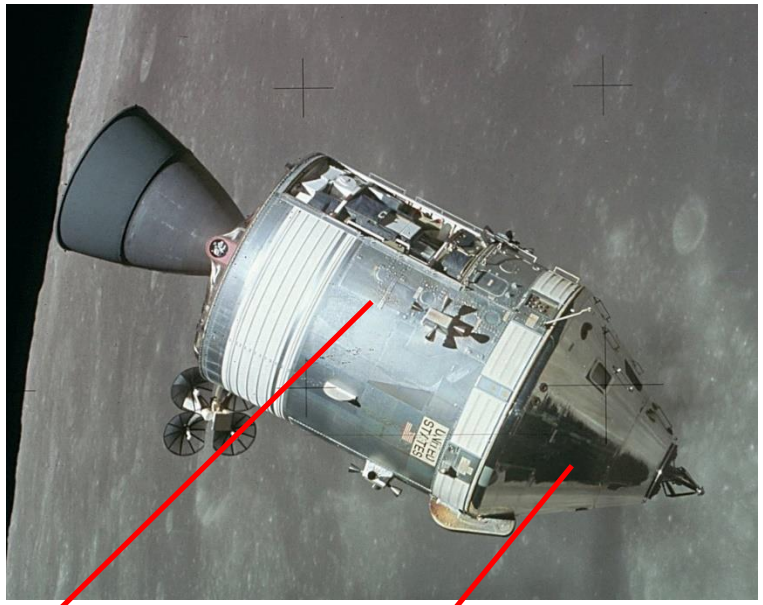
Eldon Hall was leader of the hardware design effort throughout the development of the AGC, and pioneered the use of integrated circuits (ICs) in this design.

Author of the book “Journey to the Moon”



Recent photo shared by his daughter Pam Hall

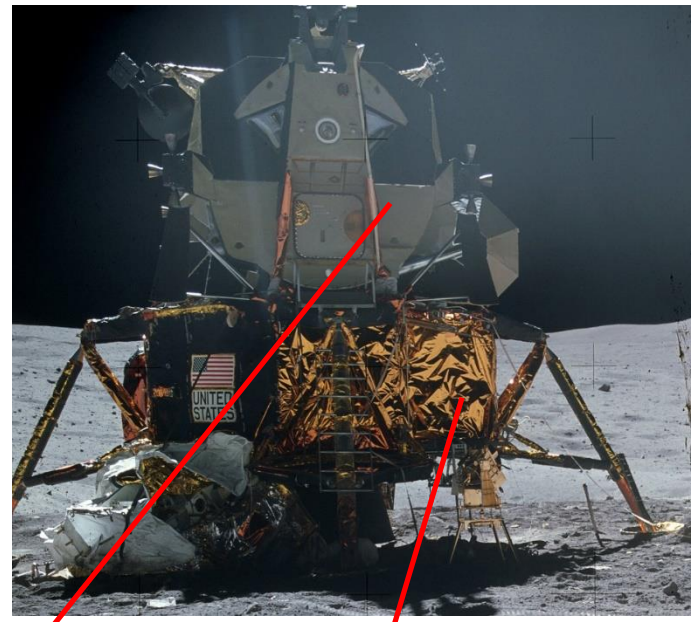
Apollo Guidance Computer



Service Module (Fuel & power cells)

Command Module (Astronaut's)

Buzz Aldrin at LM-5 left window. Apollo Guidance Computer (AGC)'s Display and Keyboard (DSKY) is at lower right.



Ascent Stage (Astronaut's)

Descent Stage (Fuel & power cells)

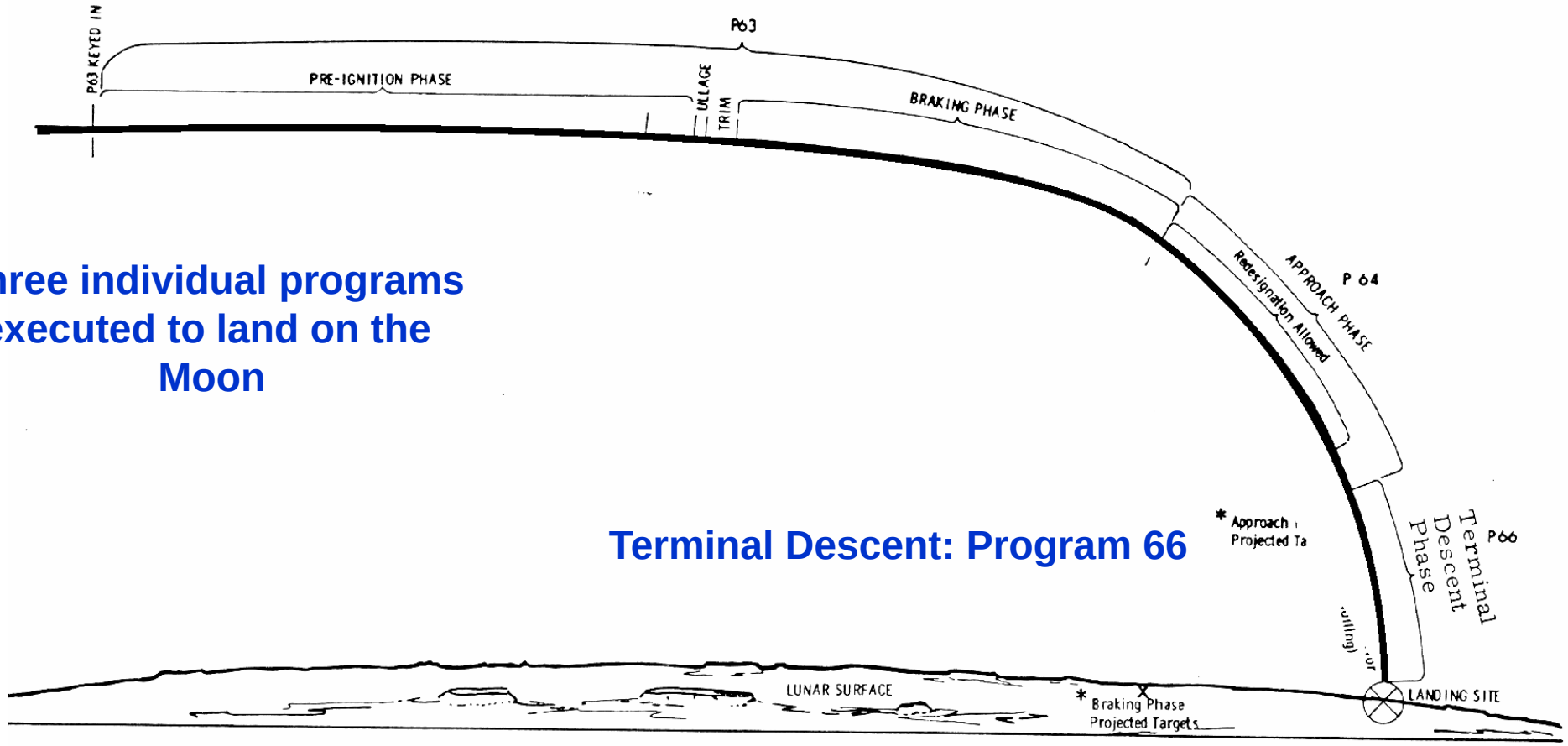
By Project Apollo Archive - AS11-36-5391, Public Domain, https://commons.wikimedia.org/w/index.php?curid=43988989

Lunar Module Descent Profile

Braking Phase: Program 63

Three individual programs executed to land on the Moon

Terminal Descent: Program 66

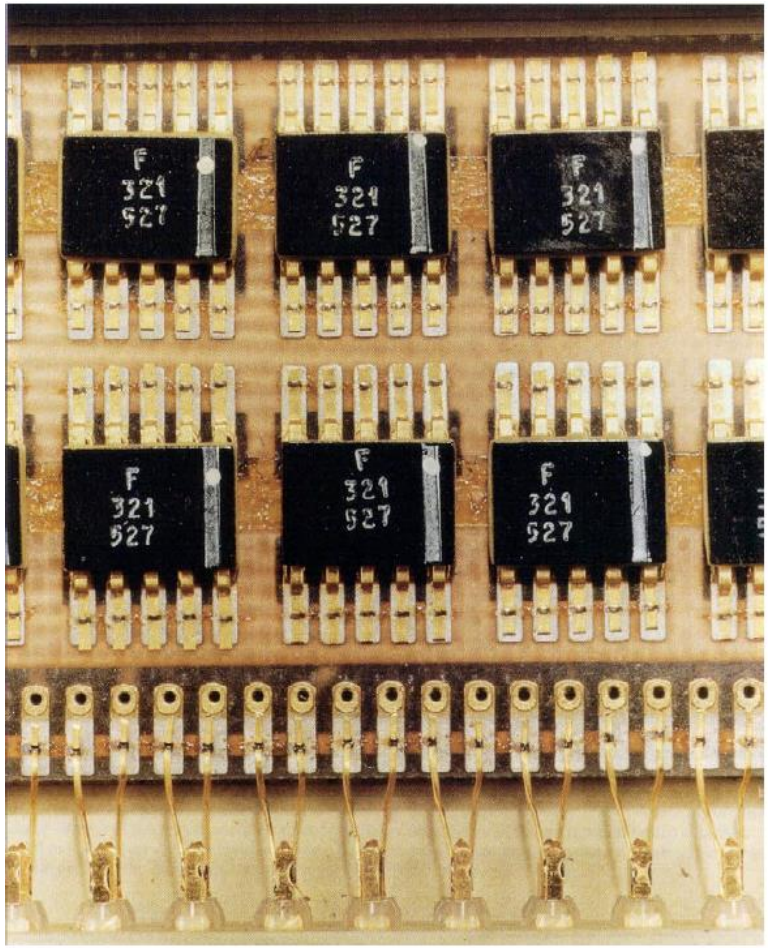


Apollo Guidance Computer (AGC) Requirements

- Autonomously navigate from the Earth to the Moon
- Continuously integrate State Vector
  - a set of data describing exactly where an object is located in space, and how it is moving
- Compute navigation fixes using stars, sun and planets
- Attitude control via digital autopilot
- Lunar landing, ascent, rendezvous
- Manually take over Saturn V booster in emergency
- Remote updates from the ground
- Real-time information display
- Multiprogramming
- Event timing at centisecond (0.01 seconds) resolution
- Multiple user interfaces (“terminals”)

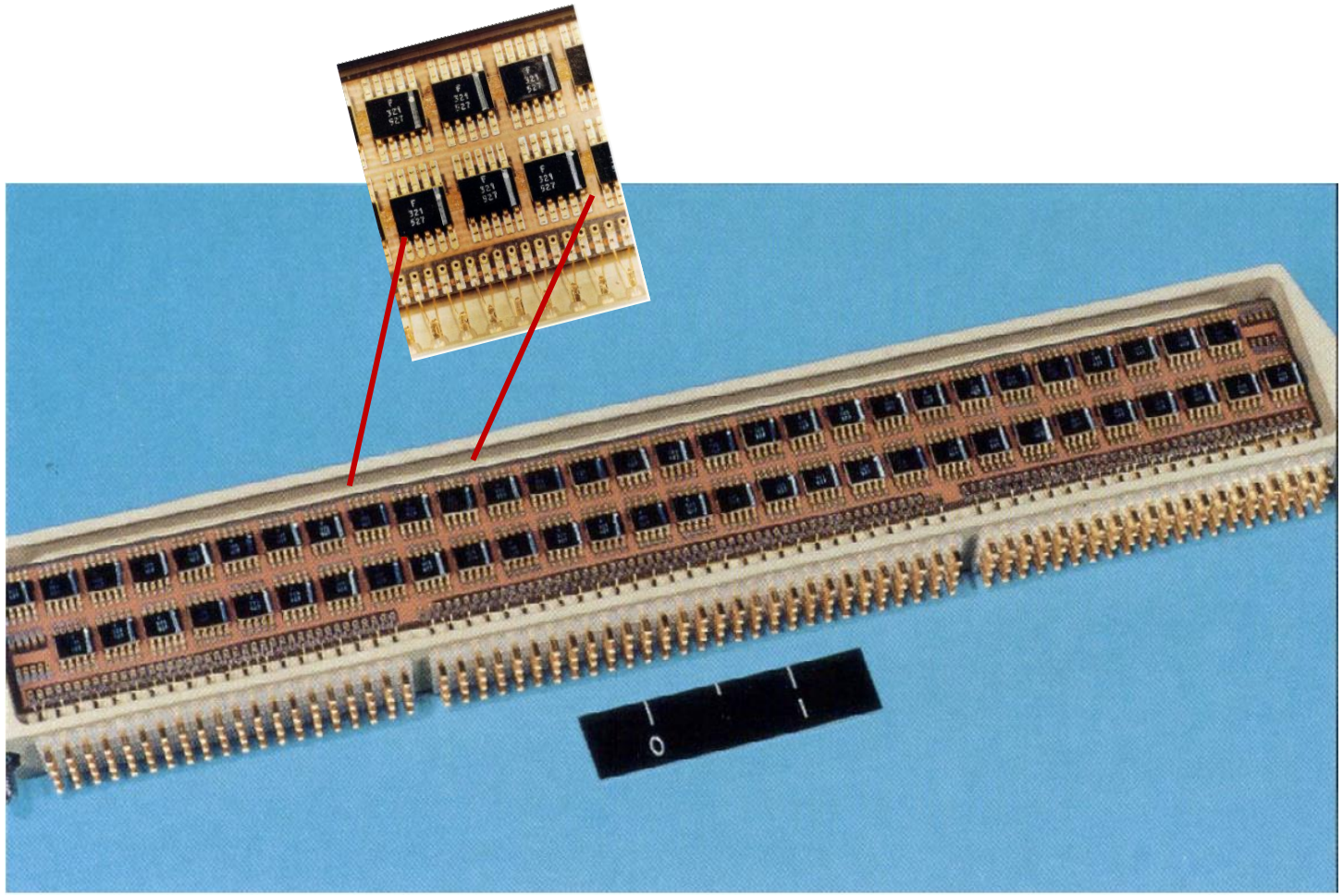
Logic Chips

- Fairchild introduced the "Micrologic" chip
  - Two triple-input NOR gates per chip
  - Resistor-Transistor Logic
- Virtually all logic implemented using the Micrologic chips
  - Single component greatly simplifies design, testing
  - Greater production quantities -> better yields and higher quality
  - Several hundred thousand chips procured (!)



“Logic Stick”

- Micrologic chips installed on “Logic Stick”
  - Subassemblies (sticks) contain 120 chips (240 gates)
  - Chips welded to multilayer boards
  - Logic boards essentially identical
  - Traditional circuit boards could not produce the necessary logic density
  - Interconnections made through wire-wraps in the underside of the “logic tray”

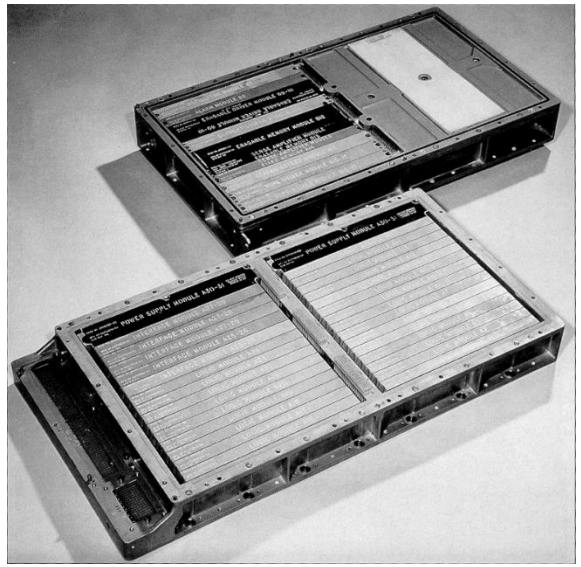


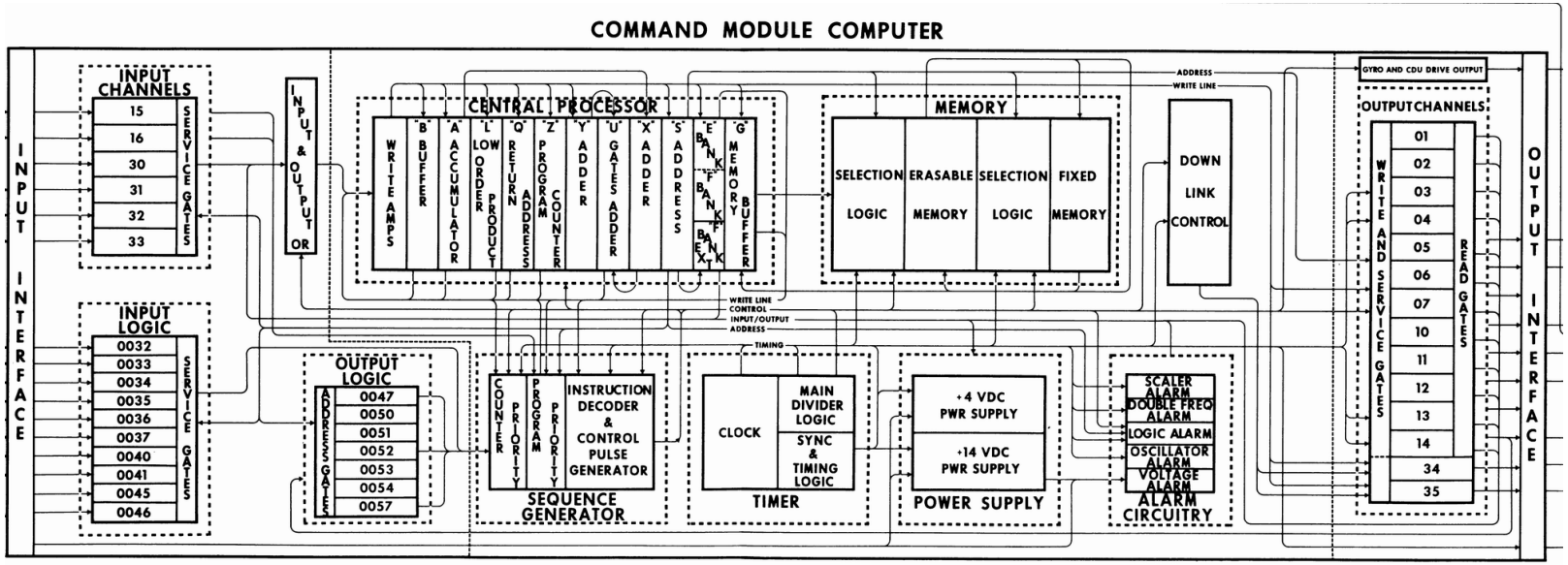
Apollo Guidance Computer Hardware

- 36K (16-bit) words ROM (core rope)
- 2k (16-bit) words core RAM
- Instructions average 12-85 microseconds
- 1 cu.ft, 70 pounds, 55 watts
- 37 “Normal” instructions
- 10 “Involuntary” instructions (Counters)
- 8 I/O instructions
- One’s complement,

  “fractional” representation

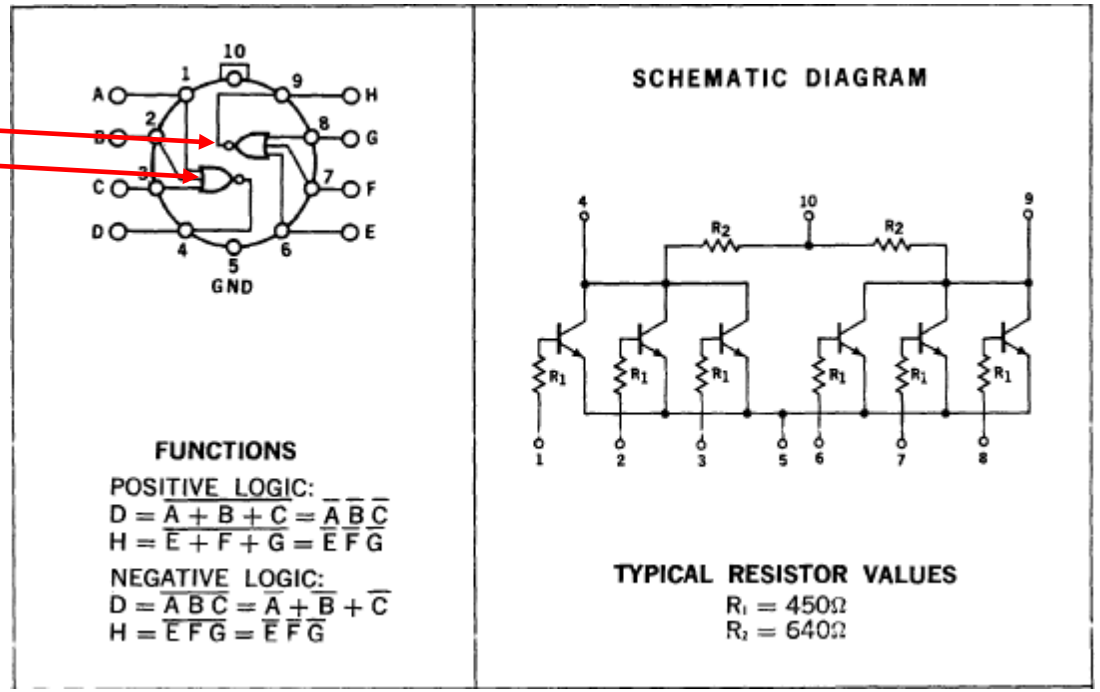
- Upper tray: Core Rope and Erasable memory
- Lower tray: Logic and interface modules



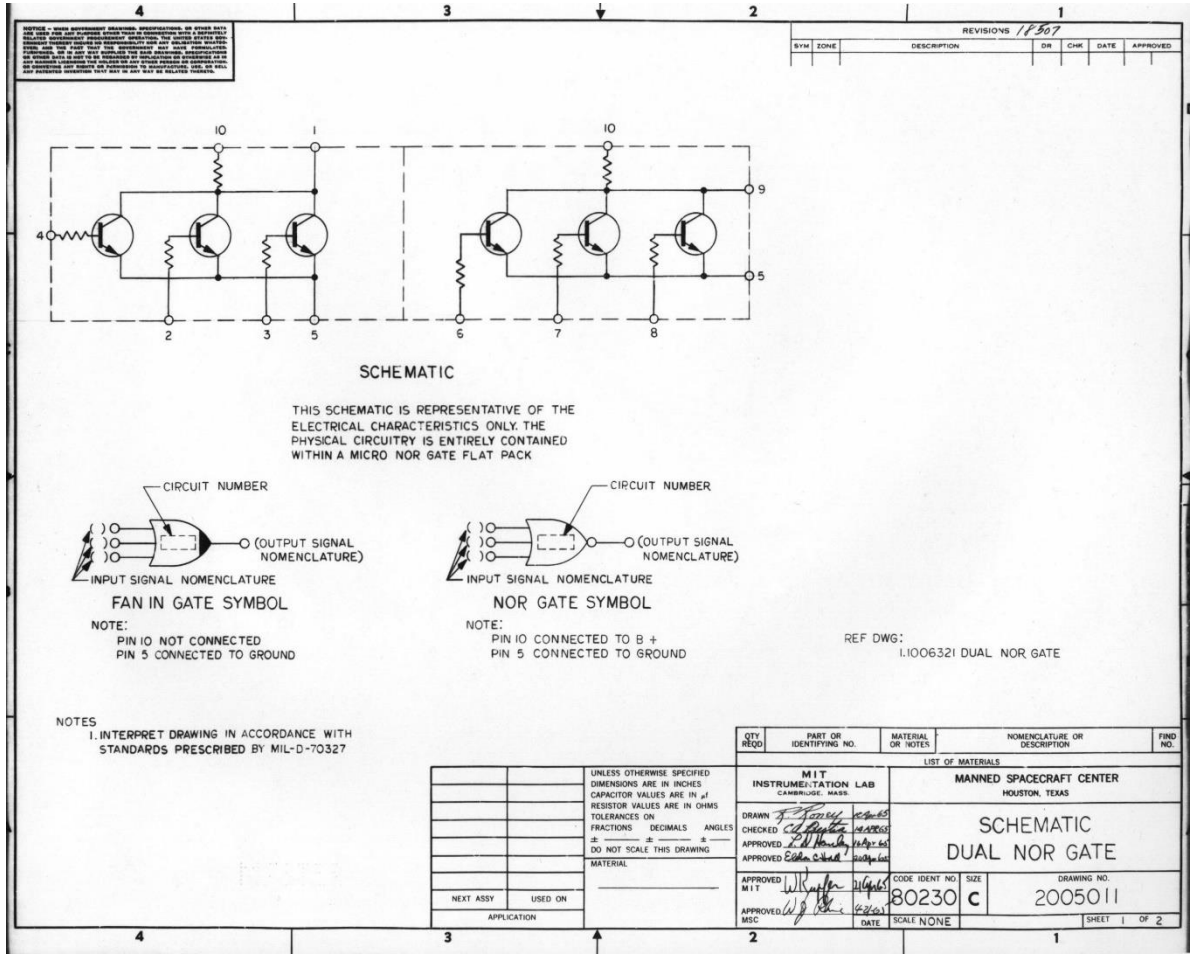


Single Logic Chip

Fairchild Semiconductor 9915 Medium Power
Dual Three Input Gate

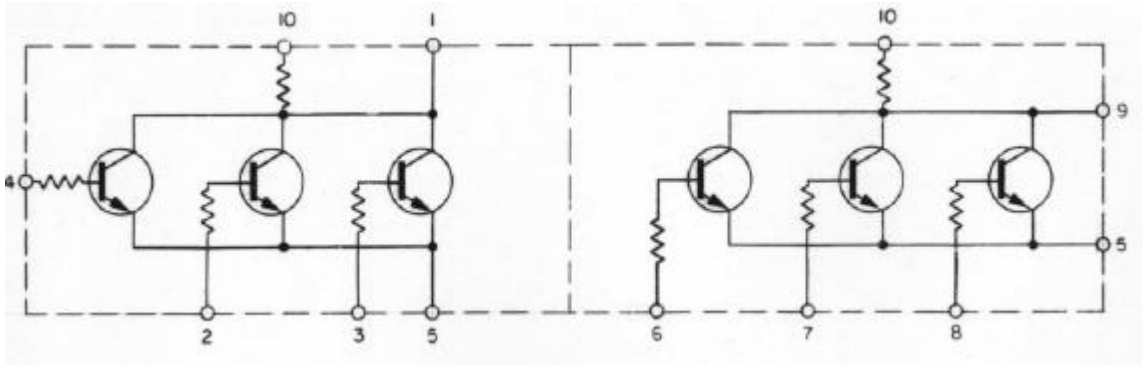


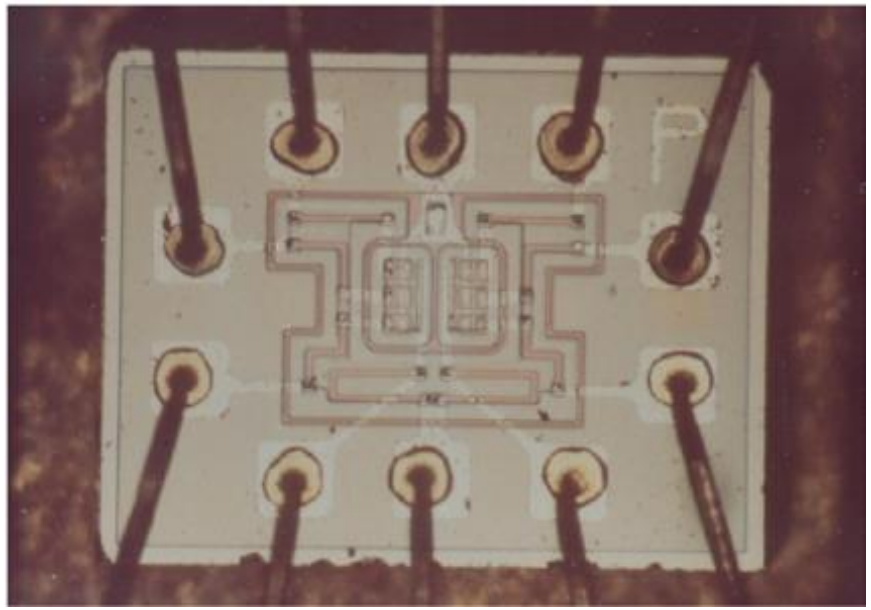
Dual NOR3 (NASA Schematic)

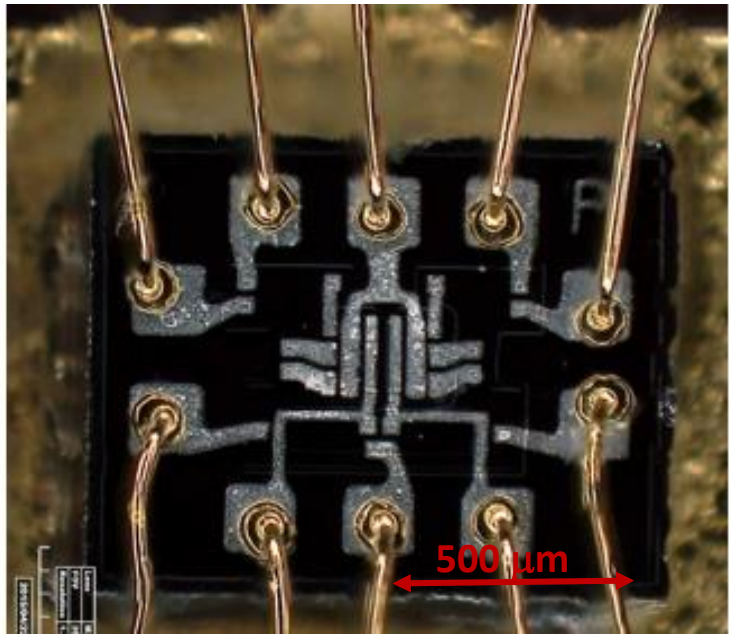


Apollo Guidance Computer NOR Gate

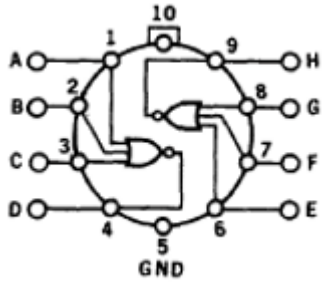
Dual NOR3 gate using Bipolar Junction Transistors

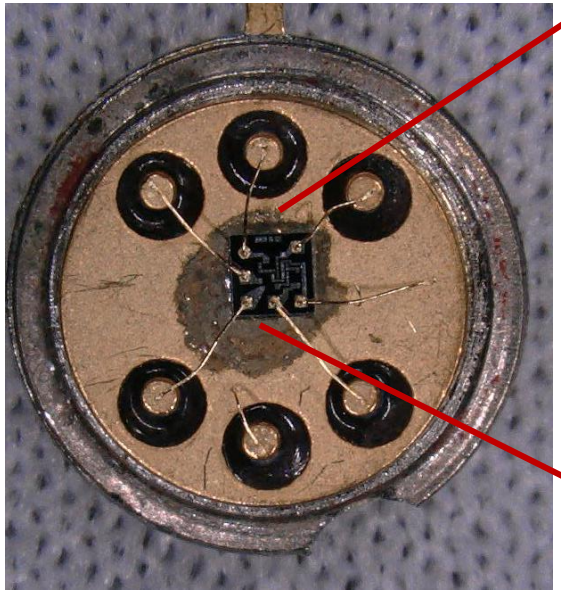




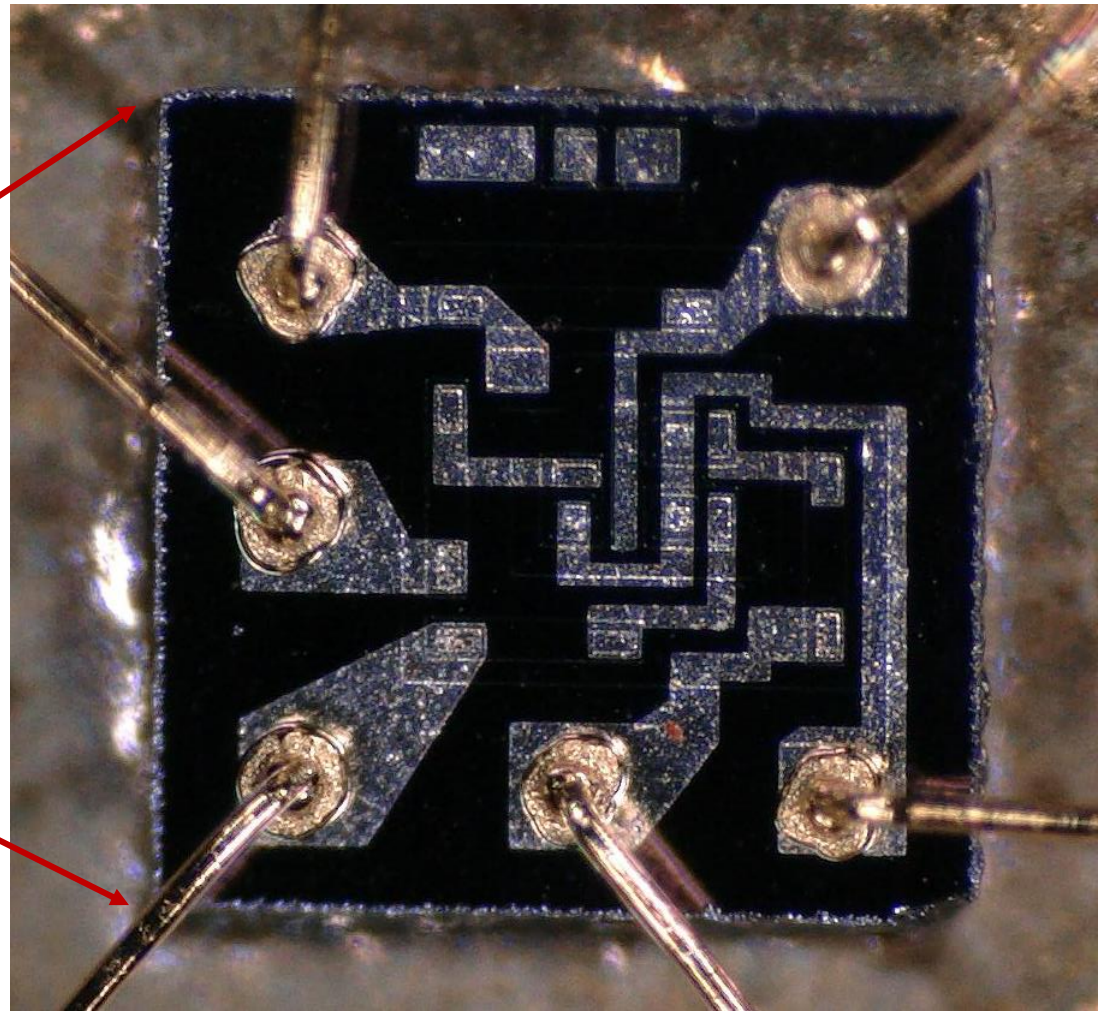


Schematic



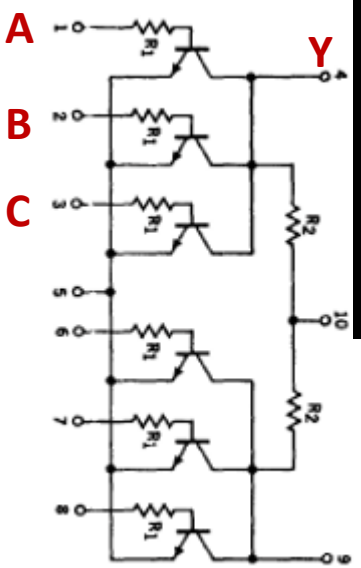


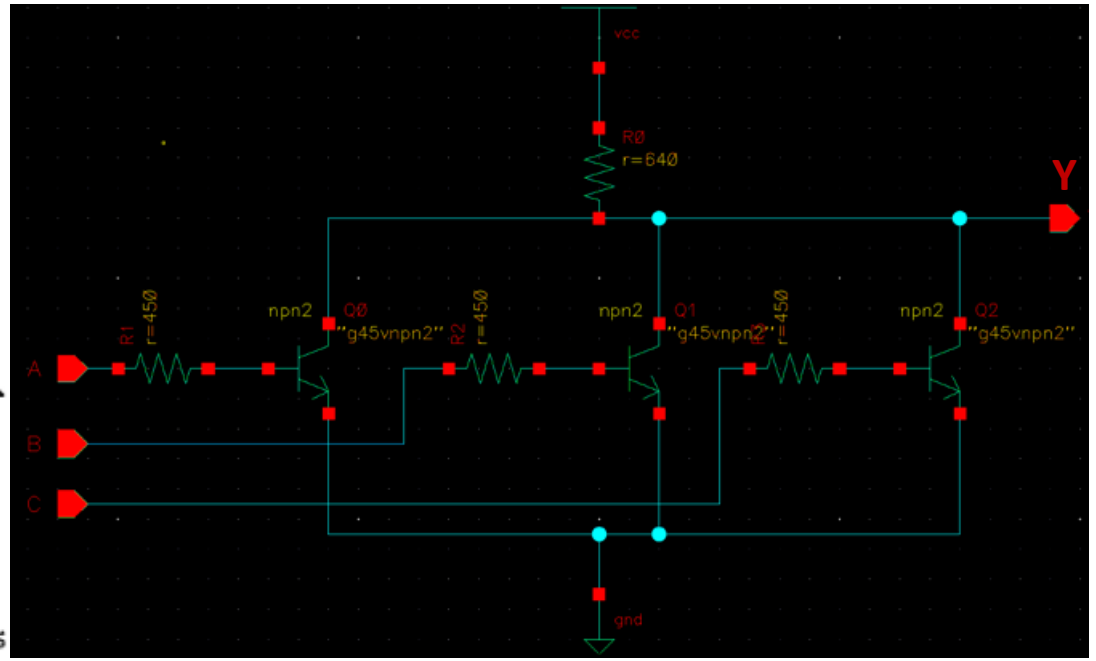
Actual Chip



3 Input RTL NOR Gate

Test Simulation





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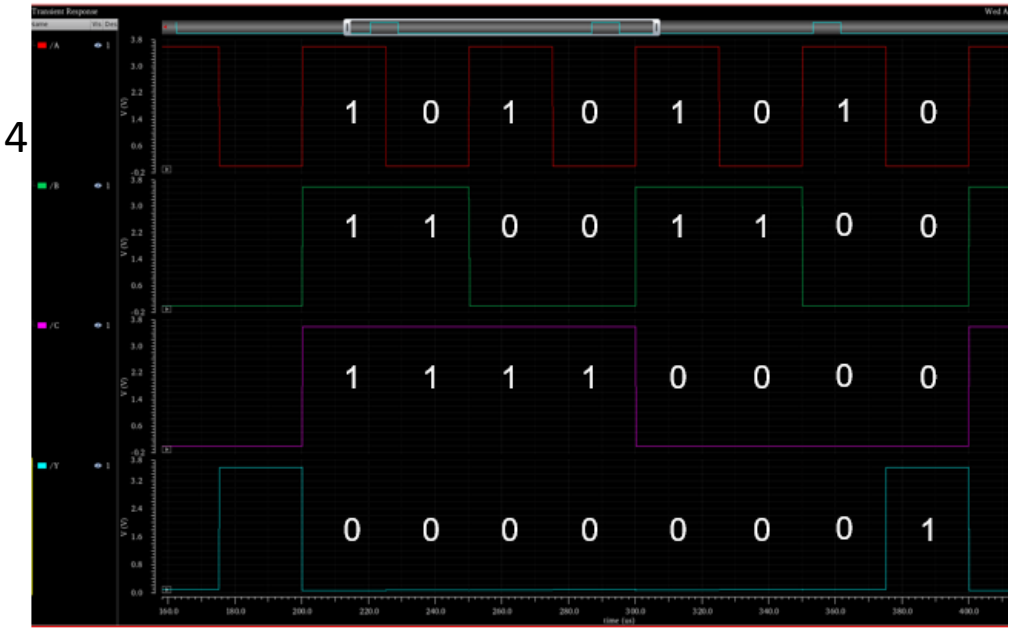
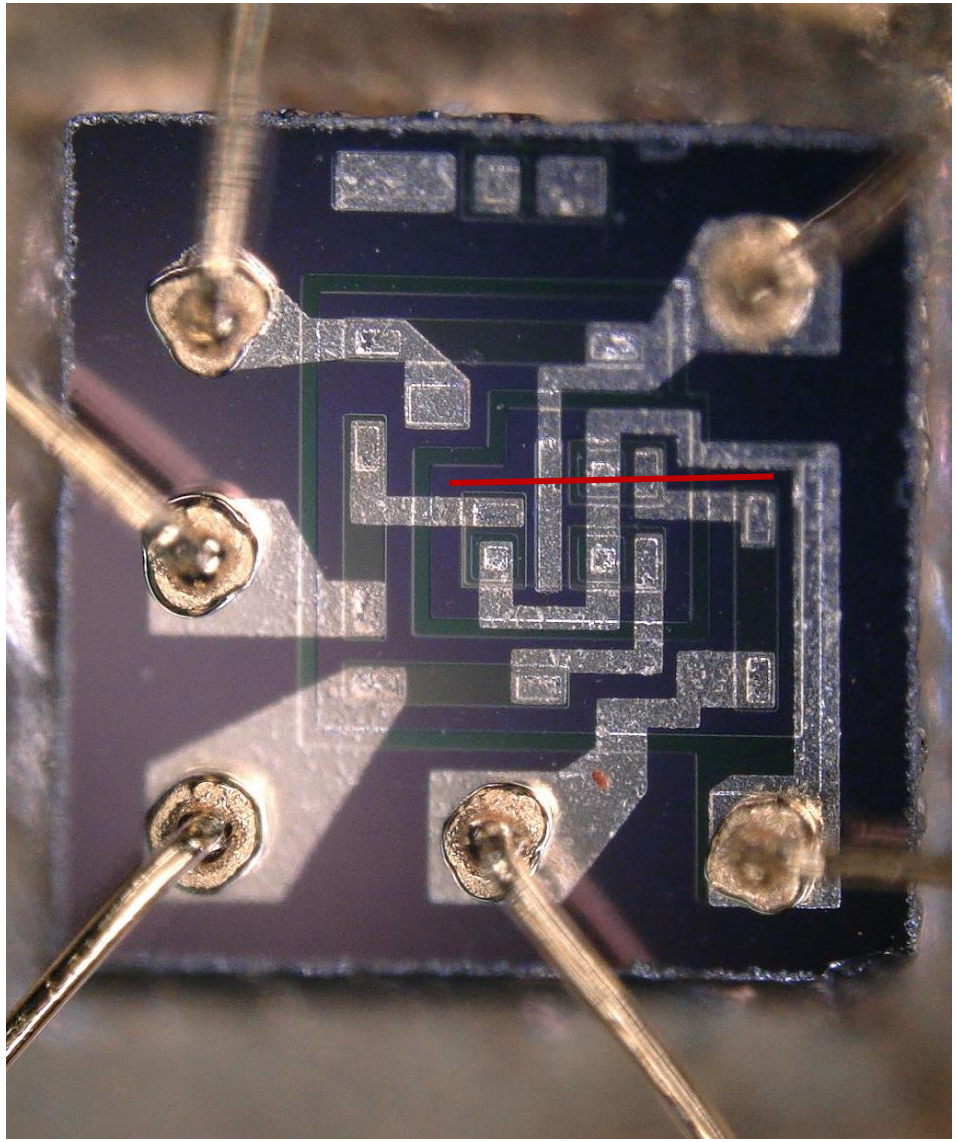
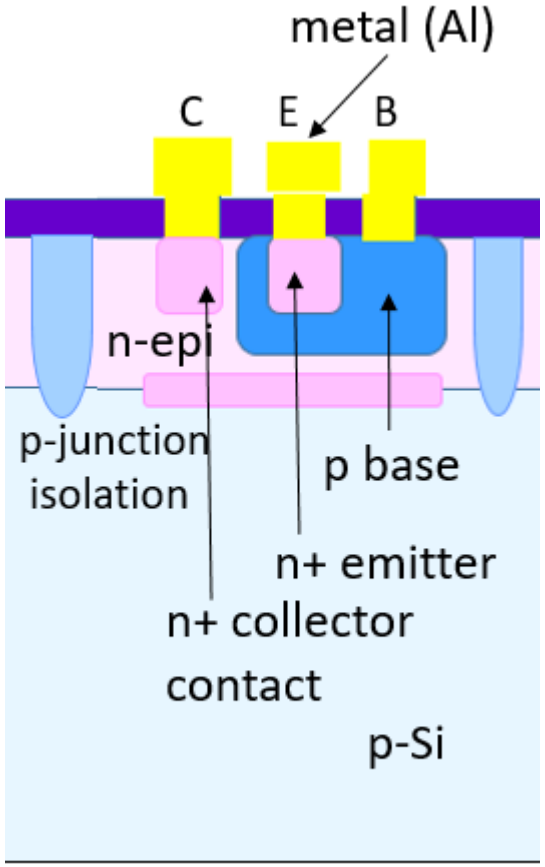


A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

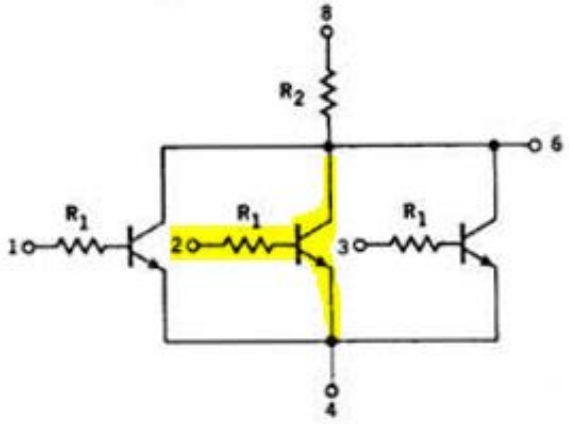
The output, Y, is true (1) if neither A nor B nor C is true. Hence, "NOR".

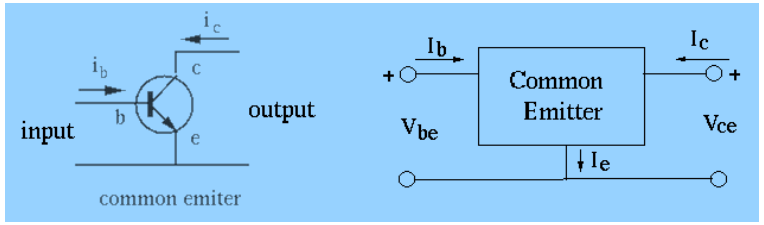
Bipolar Junction Transistor Cross Section Schematic

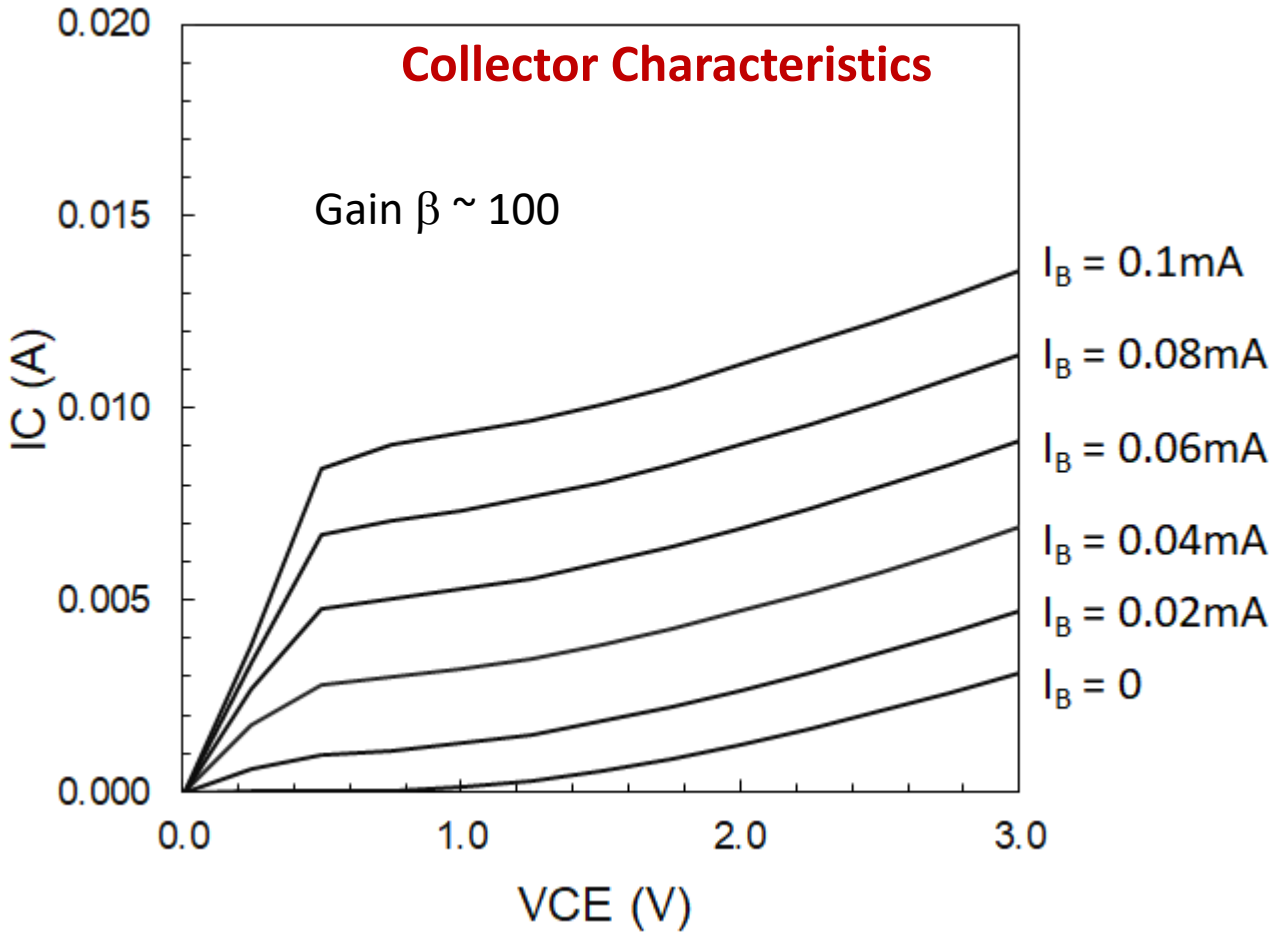




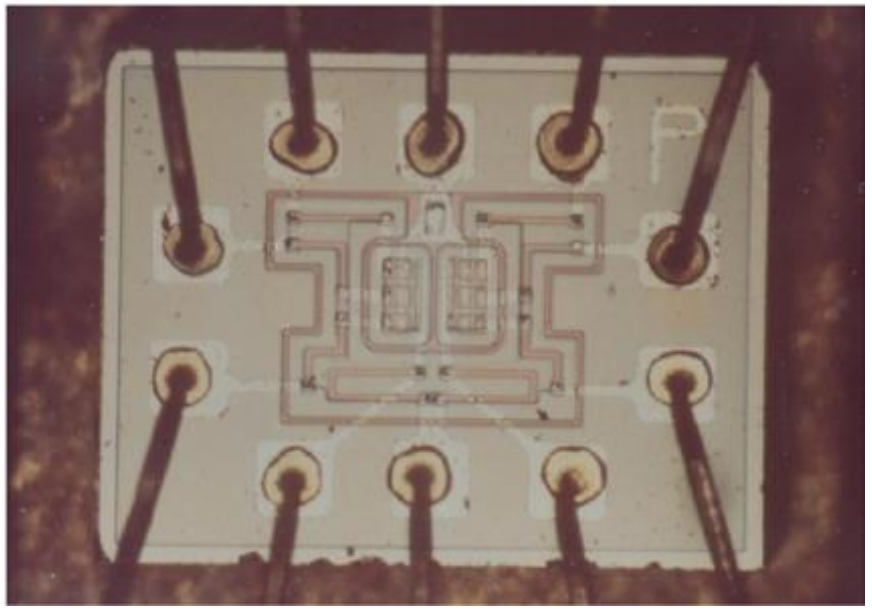
AGC Chip Transistor Testing at RIT

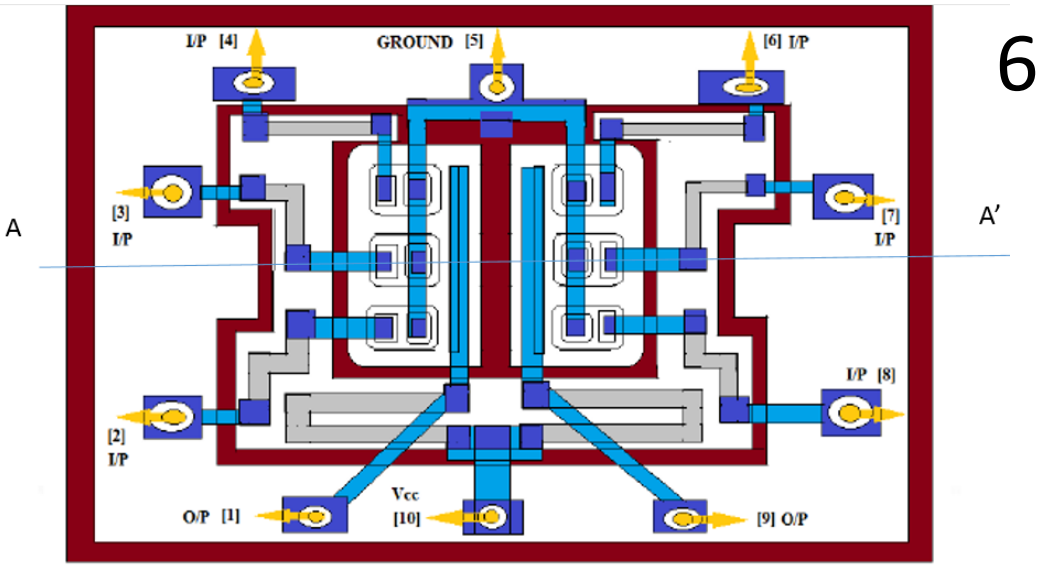






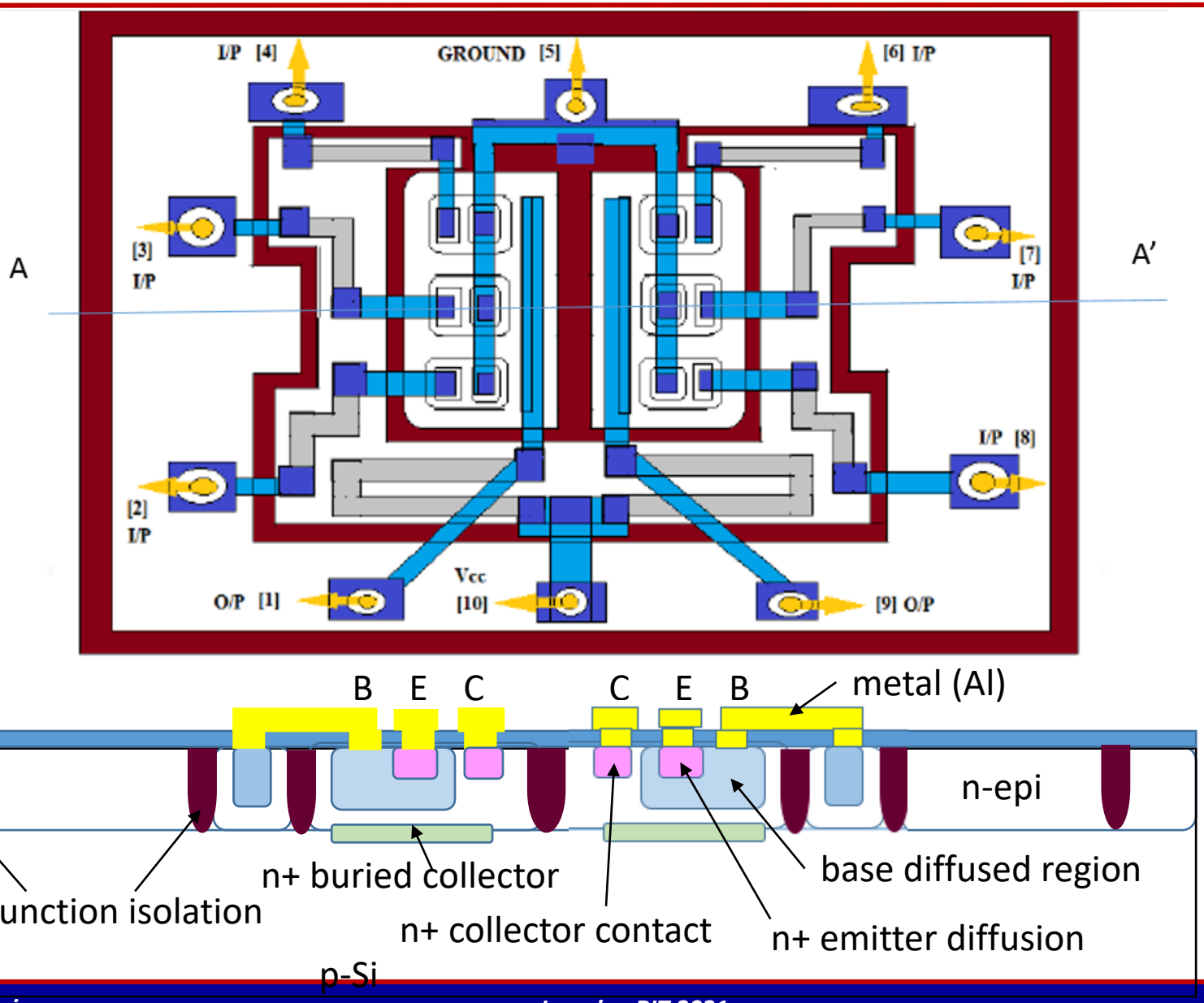
Recreating the AGC Chip



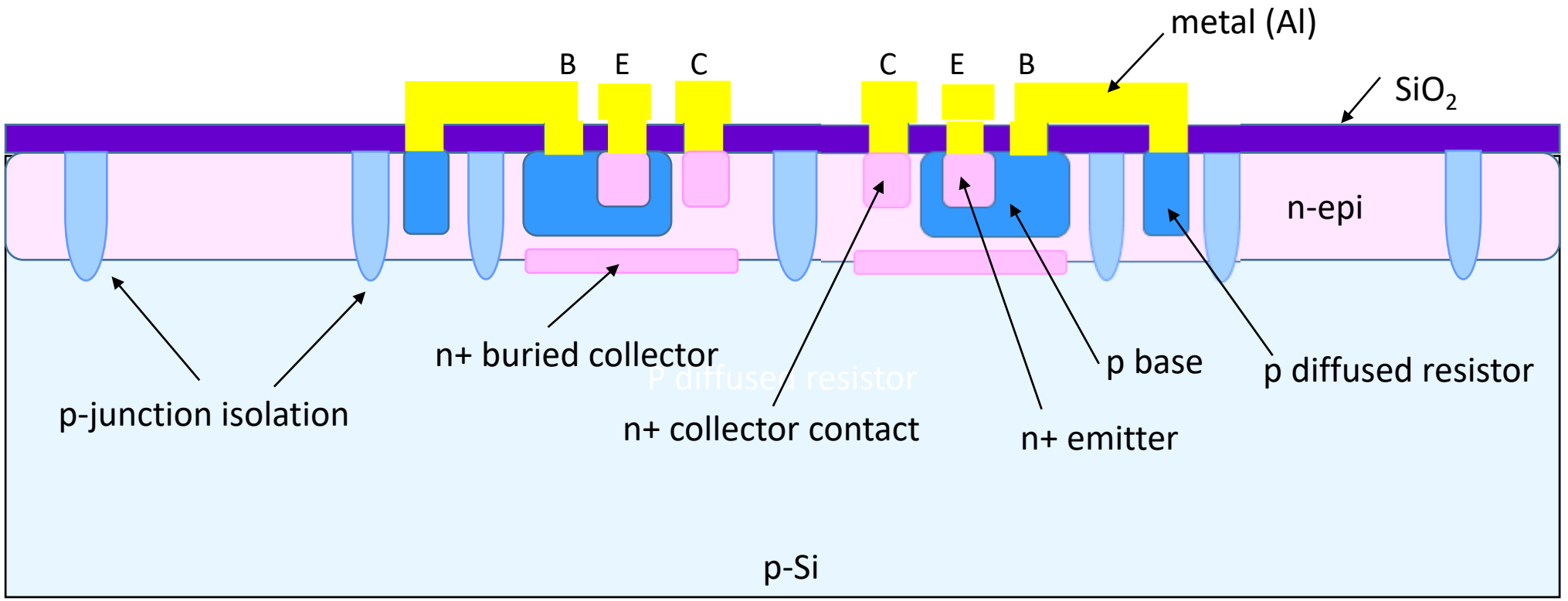


1. Explore the chip layout
2. Identify number of masking steps
3. Develop the process
4. Carry out simulations
5. Make masks
6. Run the process at RIT Microelectrnic Engineering cleanroom

Device Cross Section



Device Cross Section



Fabrication Process Flow Designed: 6 Mask Levels

Oxidation of the substrate of resistivity 10 Ω-cm

Using **Mask 1** , buried layer diffusion of Arsenic

Etch oxide layer and deposit epitaxial layer of N type silicon

Reoxidize and using **Mask 2**, isolation diffusion P-type is done to create isolated N-epi islands

Reoxidize and open windows by **Mask 3** for Boron base diffusion and for resistance diffusion

Reoxidize and open windows by **Mask 4** for Phosphorous emitter diffusion and for collector contact diffusion

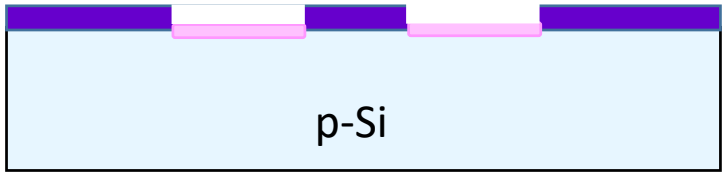
Reoxidize and open apertures by **Mask 5** for contact pads to 3 emitters, 3 bases and one elongated collector

Final metallization and using **Mask 6**, the interconnection pattern is etched

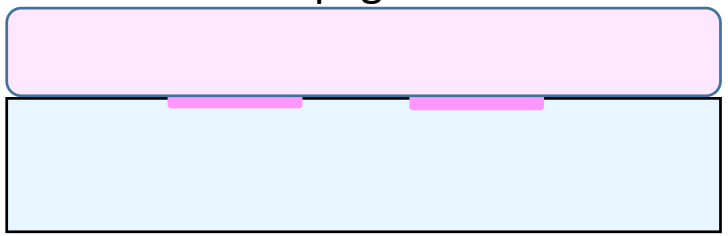
AGC Process Flow Developed

p-Si

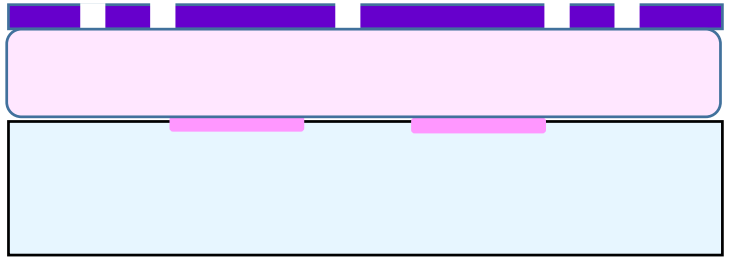
Oxide growth, Pattern, Arsenic diffusion



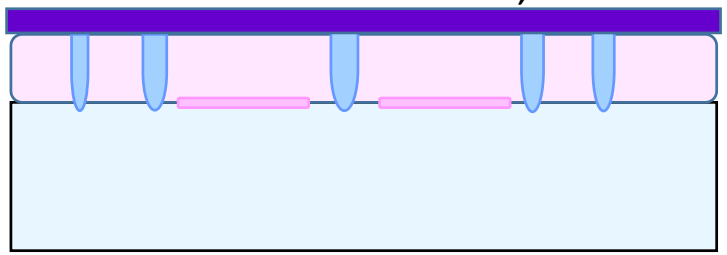
N-epi growth



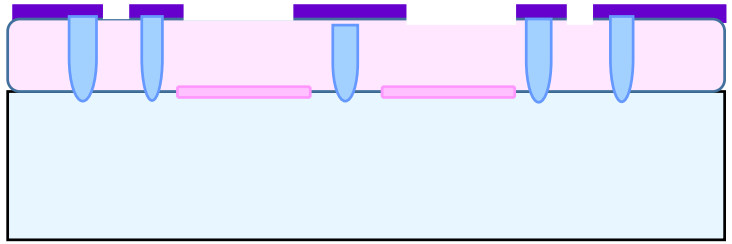
Oxidation, isolation mask



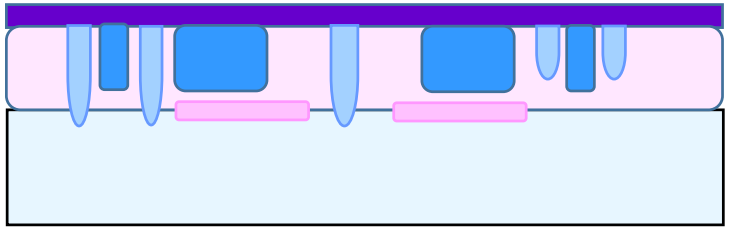
Boron diffusion & drive in, oxidation



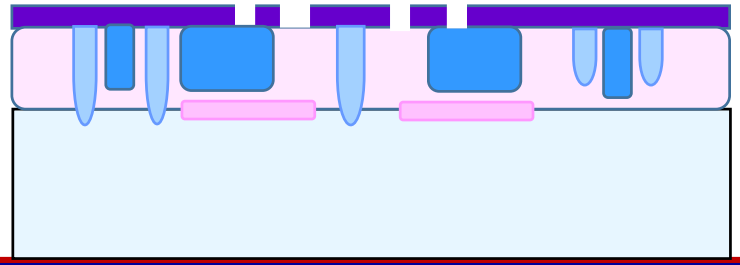
Openings for base diffusion



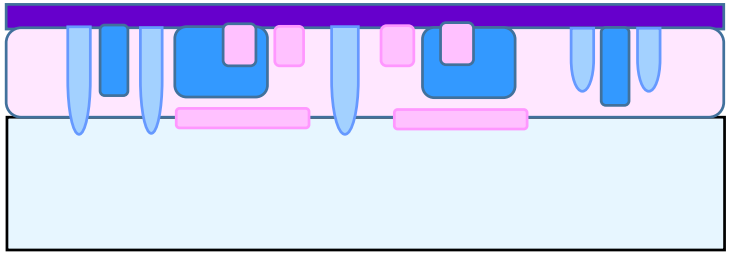
Base drive in and oxidation



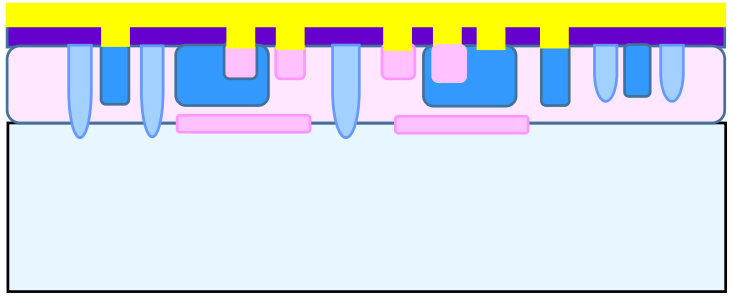
Openings for emitter diffusion



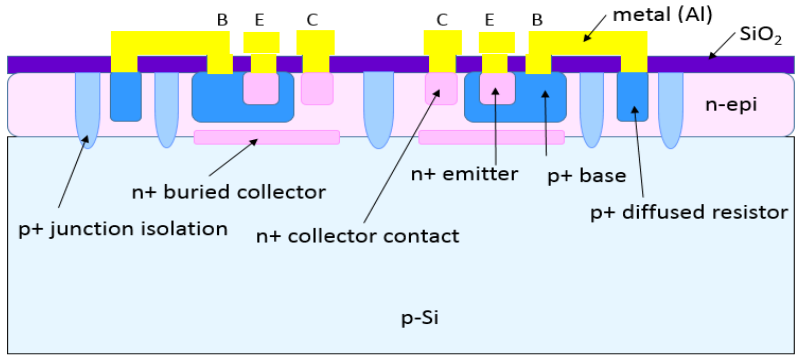
Emitter drive in and oxidation for CC



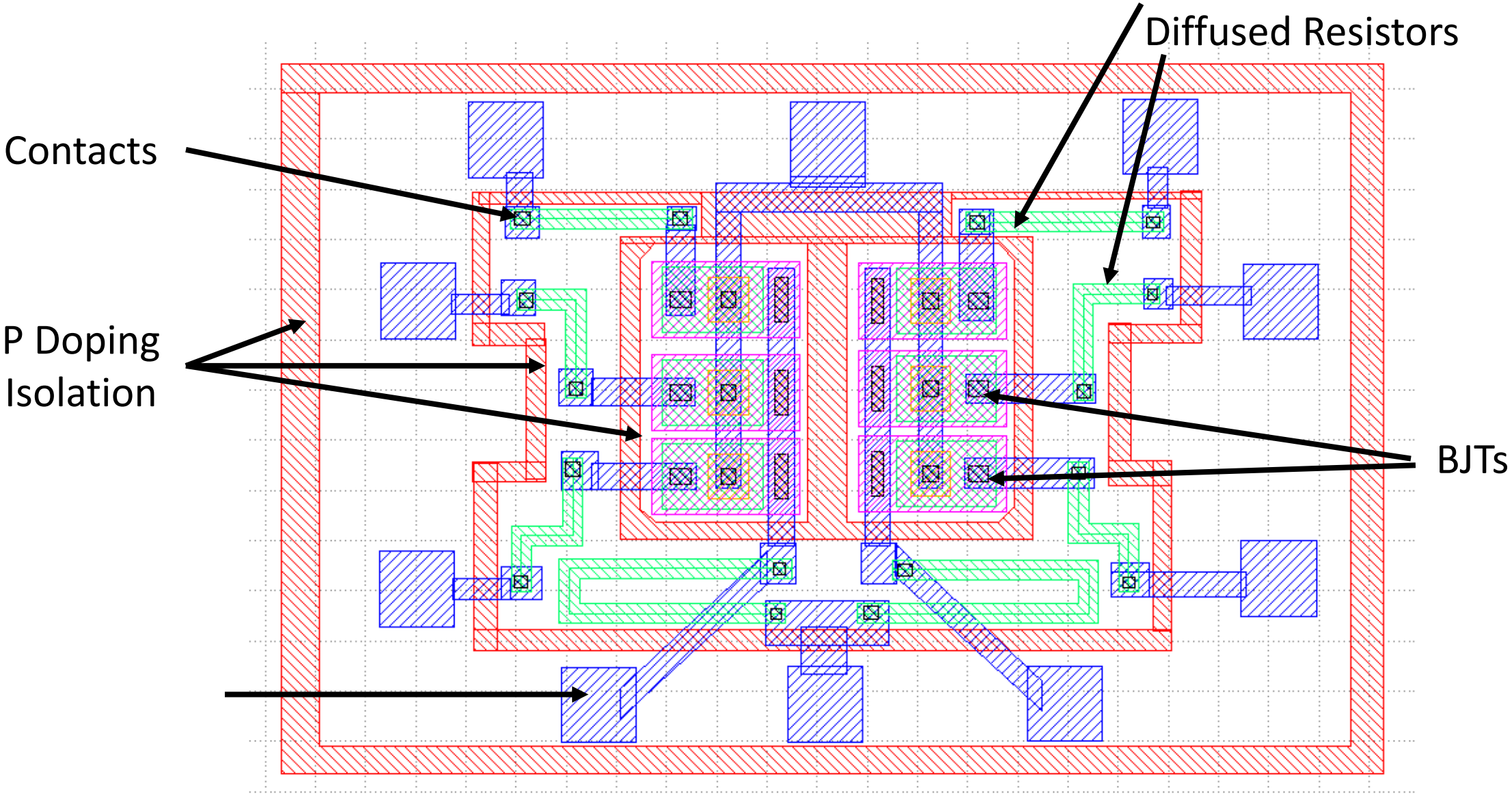
CC lithography and metal deposition



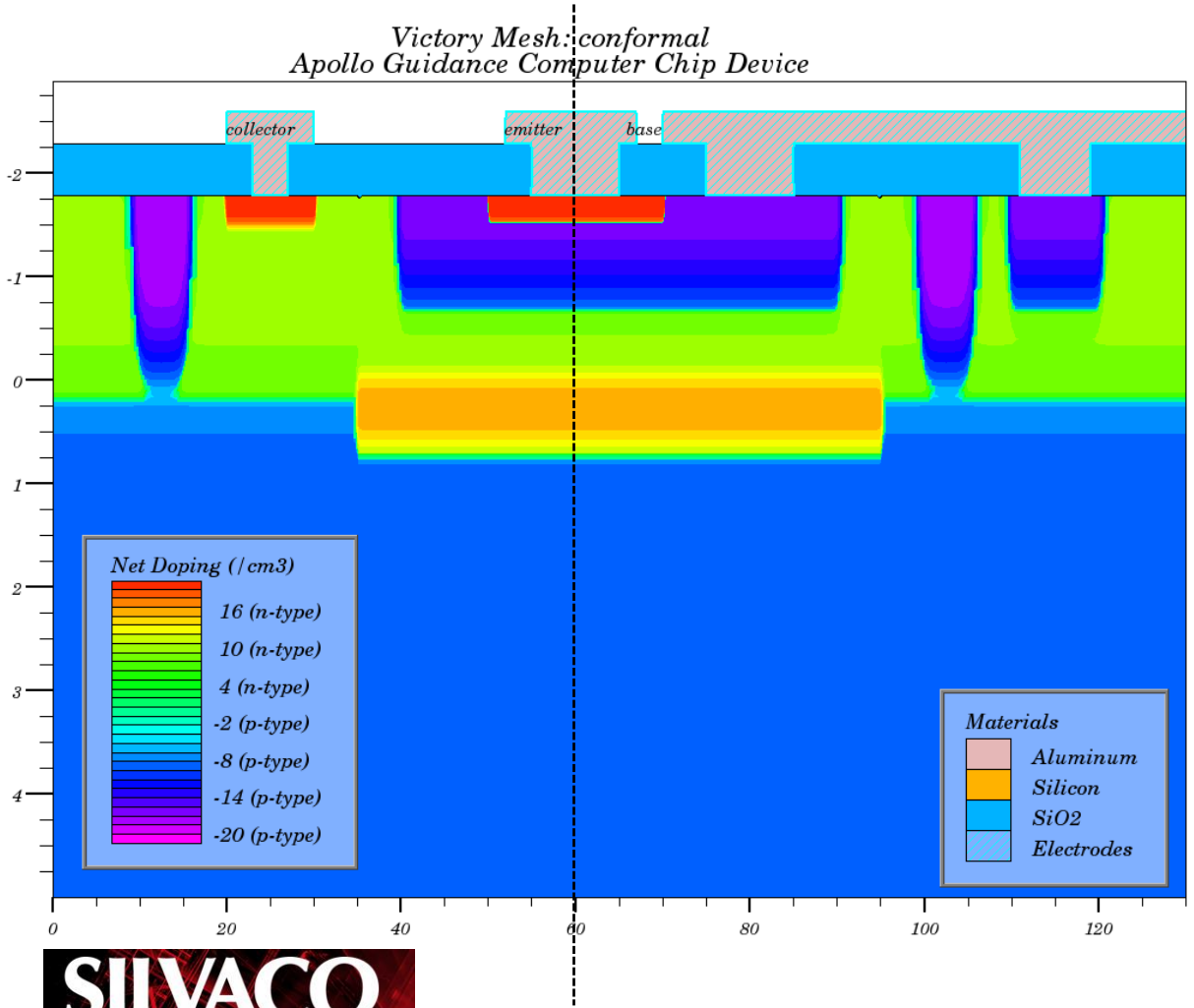
Metal patterning

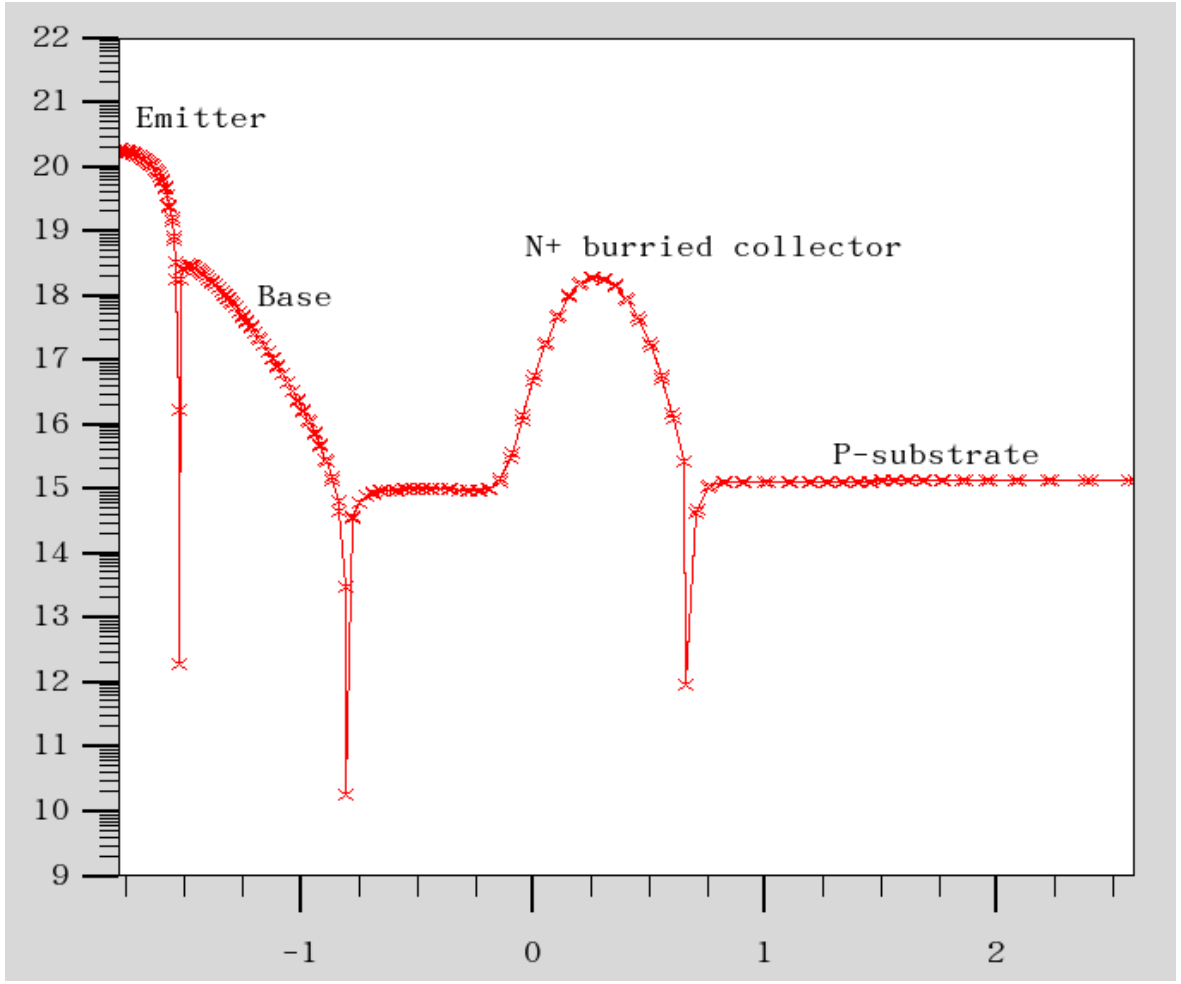


Masks Designed at RIT



Device Simulated





SILVACO
FROM ATOMS TO SYSTEMS

Exhibits the Current Gain measured on the Device

Conclusions

- We have led the creation of a team to rebuild Apollo Guidance Computer Chip in a student run fab
- The chip is tested, simulated and is being made
- Interest from a number of iconic people & institutions has been expressed to get an RIT made AGC Chip

Acknowledgments

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Rochester Institute of Technology

Udita Kapoor
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Garrett Schlenvogt, Ph.D.
US Applications Engineering Manager
Silvaco, Inc.