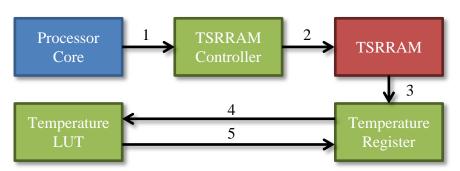
## **Technology Commercialization Opportunity**

Temperature Sensing Resistive Random Access Memory (TSRRAM)

**Technology Description:** A TSRRAM adds temperature sensing capability to resistive random access memory (RRAM) by exploiting the temperature dependence of thin-film memristors' write latency or retention time. This architecture allows a CPU to utilize its cache as a memory and an area-distributed temperature sensor concurrently.

The figure to the right illustrates one possible use case for the TSRRAM integrated into a CPU architecture as a cache memory. (1) First, a write instruction is issued by the processor core. (2) The TSRRAM controller performs any necessary address translation and starts timers in the TSRRAM. (3) The data is written to the TSRRAM. Timers in the TSRRAM capture the write time of each bit that changes, and the write times



## TSRRAM as a CPU Cache

The TSRRAM measures the temperature of every memory bit that is changed during a write instruction and stores the information in a temperature register.

are stored in a temperature register. **(4)** A pre-calibrated lookup table (LUT) is used to map timer values to temperatures. **(5)** The temperatures, write address, and system time are stored in the temperature register. The data in the temperature register can be used for dynamic thermal management. Simulation results from a subset of the SPEC2000 CPU benchmark suite indicate that the TSRRAM can sense temperatures with a mean error of ~3 K.

**Keywords:** RRAM, memristor, temperature sensor, dynamic thermal management, 3D-IC, security.

**Technology Readiness:** TSRRAM is presently at this level of readiness:

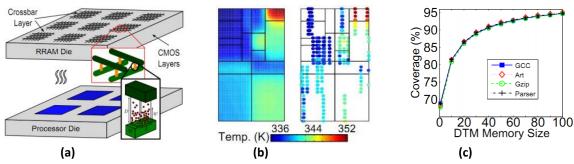
Idea Conc	<b>pt</b> Prototype	Alpha Version	Beta Version	Released
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The developers of TSRRAM will work with licensees to finalize the development and move TSRRAM towards a "released version."

Intellectual Property: TSRRAM is the subject of a US patent no. 8,750,065 which issued June 10, 2014.

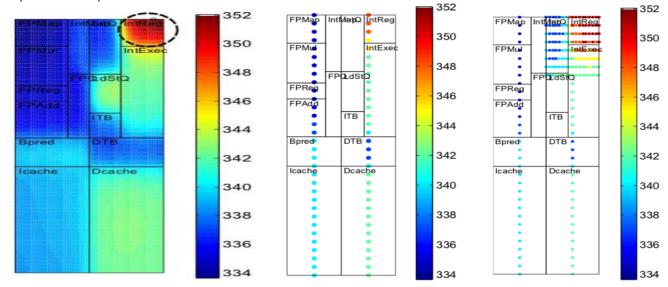
**Applications:** TSRRAM can provide accurate temperature profiles which can be used for a variety of applications, including dynamic thermal management, stand-alone temperature sensing, prevention of power or temperature-based side channel security attacks, on-chip security, reliability management, IC testing, and hardware security/Trojan detection and energy efficient 3D-IC designs.





## Passive Sensing in 3D-IC MPSoCs

The TSRRAM architecture relays several temperature data points associated with every write instruction. If the write instructions are random enough, then the TSRRAM can provide a dense, accurate temperature profile of the chip. (a) TSRRAM (RRAM die) fabricated on top of a processor die. This 3D architecture allows the TSRRAM to sense the temperature of the processor cores below it. (b) Example temperature data points collected from the GCC benchmark (SPEC2000 CPU benchmark suite). On the left is the thermal profile of an Alpha 21364 core running the benchmark. On the right is the temperature data returned from the TSRRAM. (c) A high coverage of hotspots is possible if enough temperature data points are saved.



## **Active Sensing in 3D-IC MPSoCs**

The TSRRAM architecture can also be used to actively sense chip regions of interest. One possible example of this is iteratively scanning on-chip temperatures to find a global chip hotspot. In the figure above, a thermal profile (left) is shown with a global hotspot (circled). In the first iteration (middle) temperature measurements are taken with low spatial sampling frequency. In the next iteration (right), a higher sampling frequency is used in the hottest region, giving an accurate representation of the global hotspot region.

Target Customers: Memory Mfgs, IC Industries, Cyber Security Systems Mfgrs (use chip images)

**Opportunity:** RIT's Intellectual Property Management Office (IPMO) is interested in working with those parties who are qualified and interested in the commercialization of TSRRAM. Arrangement types include licensing as well as performing R&D under a sponsored research program.

**Contact:** Those interested in learning more about this opportunity should contact: **Mr. William E. Bond**, Director of Intellectual Property Management at RIT (585) 475-2986 <a href="mailto:bill.bond@rit.edu">bill.bond@rit.edu</a> Please refer to ID 2011-019-01/11-16

