Andrew C. Estroff

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EDUCATION:

Rochester Institute of Technology, Rochester NY
Microelectronic Engineering, Bachelor of Science, May, 2003
Microsystems Engineering, PhD, Expected 2009

COURSEWORK:

Microlithography Systems, Microlithography Materials, Geometric Optics, Modern Optics for Engineers, Quantum Electronics, Holography, Electromagnetic Fields, Theoretical Methods, Linear Image Mathematics, Micro-Optics, Micro and Nano-Photonics, MEMS Design and Manufacturing, Systems Engineering, Polymer Science, Materials Physics and Technology for Nanoelectronics, Quantum Physics, Remote Sensing

RESEARCH INTERESTS:

193nm and 248nm lithography (immersion and dry), mask aligners, contact/proximity printing, VLSI, semiconductor processing technology (thin and thick film deposition/coating, metrology, sputtering, evaporation, CVD, CMP, SEM, ion implant, diffusion, thermal processing, oxide growth, wet and dry RIE/plasma etching)

WORK HISTORY:

Center for Nanolithography Research, RIT, Rochester, NY 09/06-Present
Hybrid Projection-Interferometric Lithography for Nano-patterning, Research Assistant

Research related to novel double patterning techniques comprised of forming an interferometric grating in resist using methods learned from stimulated emission depletion fluorescence microscopy (STED) and forming a custom pattern using a projection lithography trim step. Teaching assistant for Lithography Materials and Processes as well as Lithography Systems.

Interuniversity MicroElectronics Center (IMEC), Leuven, Belgium 01/05-08/06
International Scholar

Examination of mask topography effects, 1- and 2-D mask induced polarization through experiment and simulation, and double patterning techniques for sub-45nm technologies.

Mentor Graphics Corporation, San Jose, CA 01/05-08/06
Assignee to IMEC

Calibration and verification of OPC models for immersion lithography and polarized sources, verification of 3-D mask polarization models for OPC, application of OPC in double patterning for sub-45nm technologies

Center for Nanolithography Research, RIT, Rochester, NY 09/03-01/05
Mask Induced Polarization Effects, Research Assistant

Research related to mask induced polarization effects; presented at SPIE in 2004 and 2005, and SRC in 2004 and 2005, published in JM3. Additional research related to immersion lithography. Teaching assistant for the introductory freshman lithography course.

IBM, Burlington, VT 06/02-11/02
Process Engineer, DUV Lithography

Implemented defect monitoring, classification, and reduction on 193nm and 248nm lithography production lines. Assisted in developing a process to eliminate resist line collapse at dimensions sub-0.13 micrometers. Statistical process control to ensure process capability.

Microelectronics Department, RIT, Rochester, NY 06/01-08/01
Resonant Interband Tunneling Diodes Research, Coop

Research related to the integration of Resonant Interband Tunneling Diodes (RITDs) with standard CMOS processes. Presented at RIT's Undergraduate Research Symposium. Assisted in setting up a science curriculum for middle school students based on semiconductors.

Microelectronics Department, RIT, Rochester, NY 12/00-05/01
Laboratory Assistant

Taught freshman introductory lab course requiring the students to design, build, and test poly-Si resistors.

Karl Suss America, Waterbury Center, VT 05/00-11/00
Applications Engineer

Acceptance testing of lithography coating clusters at Karl Suss and customer sites, lithography process development for KSA and customers, created template for technical notes/papers, 70μm and 100μm single coat photoresist projects, and metrology tool gauge studies.

Microelectronics Department, RIT, Rochester, NY 09/99-05/00
Cleanroom Technician

Equipment/tool maintenance and testing, maintenance of wet benches, management of solvents, bases, and other chemicals, testing of air quality, and general upkeep of facilities

PROJECTS:

Alternating Phase Shifting Mask for DUV Lithography 01/03-05/03
Senior Research Project, RIT, Rochester, NY

Design, fabrication, and characterization of mask set, comparison between standard profilometry and atomic force microscopy for characterization of etch depth/phase shift, and correlation between phase shift and printed line in photoresist.

Wafer Scale Packaging 12/00-05/01
RIT, Rochester, NY

Process engineering work related to wafer bumping.

AWARDS AND ACTIVITIES:

Dean's List: 1998-2003

RIT Presidential, Alumni Scholarships: 1998-2003

RIT Orchestra: 1998-present