

# Self-Anchored Catalyst Interface Enables Ordered Via Array Formation from Submicrometer to Millimeter Scale for Polycrystalline and Single-Crystalline Silicon

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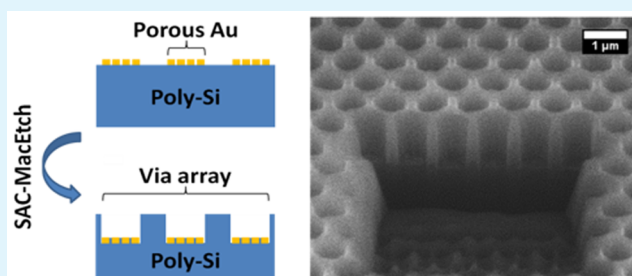
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## Supporting Information

**ABSTRACT:** Defying text definitions of wet etching, metal-assisted chemical etching (MacEtch), a solution-based, damage-free semiconductor etching method, is directional, where the metal catalyst film sinks with the semiconductor etching front, producing 3D semiconductor structures that are complementary to the metal catalyst film pattern. The same recipe that works perfectly to produce ordered array of nanostructures for single-crystalline Si (c-Si) fails completely when applied to polycrystalline Si (poly-Si) with the same doping type and level. Another long-standing challenge for MacEtch is the difficulty of uniformly etching across feature sizes larger than a few micrometers because of the nature of lateral etching. The issue of interface control between the catalyst and the semiconductor in both lateral and vertical directions over time and over distance needs to be systematically addressed. Here, we present a self-anchored catalyst (SAC) MacEtch method, where a nanoporous catalyst film is used to produce nanowires through the pinholes, which in turn physically anchor the catalyst film from detouring as it descends. The systematic vertical etch rate study as a function of porous catalyst diameter from 200 to 900 nm shows that the SAC-MacEtch not only confines the etching direction but also enhances the etch rate due to the increased liquid access path, significantly delaying the onset of the mass-transport-limited critical diameter compared to nonporous catalyst c-Si counterpart. With this enhanced mass transport approach, vias on multistacks of poly-Si/SiO<sub>2</sub> are also formed with excellent vertical registry through the polystack, even though they are separated by SiO<sub>2</sub> which is readily removed by HF alone with no anisotropy. In addition, 320 μm square through-Si-via (TSV) arrays in 550 μm thick c-Si are realized. The ability of SAC-MacEtch to etch through poly/oxide/poly stack as well as more than half millimeter thick silicon with excellent site specificity for a wide range of feature sizes has significant implications for 2.5D/3D photonic and electronic device applications.

**KEYWORDS:** high aspect ratio, polycrystalline silicon via, MacEtch, self-anchored catalyst, through-Si-via



## INTRODUCTION

Metal-assisted chemical etching (MacEtch) is a local electrochemical etching that is capable of producing high aspect ratio (HAR) semiconductor structures in a simple chemical solution at near room temperature. This allows elimination of high energy ion induced damage of surfaces and side wall scallops that

typically occur in conventional deep reactive ion etching.<sup>1,2</sup> Photonic and electronic device applications of MacEtched

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structures have been demonstrated including light emitting diodes (LEDs),<sup>3</sup> solar cells,<sup>4–6</sup> biosensors,<sup>7</sup> supercapacitors,<sup>8</sup> thermoelectrics,<sup>8,9</sup> and FinFETs.<sup>10</sup>

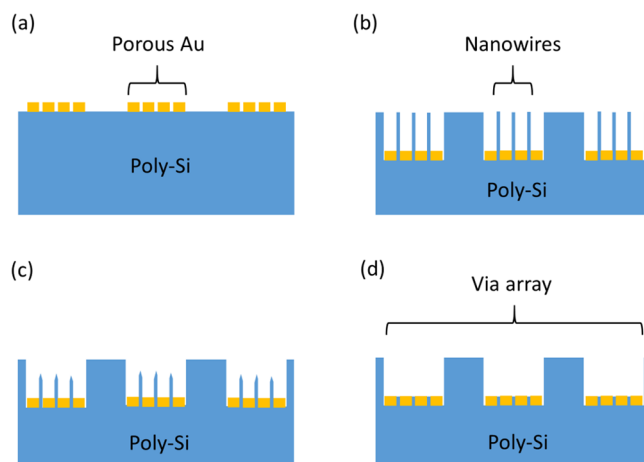
Typical Si MacEtch starts by depositing a noble metal film (e.g., Au, Pt, Ag, Ir, or even graphene)<sup>11–14</sup> as the catalyst on the substrate. The catalyst can be patterned into any arbitrary shapes such as dots, meshes, boomerangs.<sup>15</sup> Then the sample is immersed in a solution mixture of acid (e.g., HF) and oxidant (e.g., H<sub>2</sub>O<sub>2</sub>, Fe(NO<sub>3</sub>)<sub>3</sub>, KMnO<sub>4</sub>) to selectively oxidize and etch the Si localized under the catalyst film. Local cathodic and anodic reactions take place during MacEtch, where holes are generated by the reduction of oxidant (cathodic reaction) at the liquid/catalyst interface and injected into the valence band of Si to form the oxidized Si that is subsequently etched by HF (anodic reaction). The steps that involve the hole generation, injection, and diffusion are referred to as the carrier generation process (CG), while the removal of the oxidized Si is referred to as the mass transport (MT) process.<sup>16</sup> It has been shown that the maximum etch rate takes place when CG and MT are balanced, which ensures minimum lateral movement of the catalysts.

HAR ordered single-crystalline Si (c-Si) structures such as nanowires (NWs), fins, and via arrays have been demonstrated using MacEtch. The etch rate, etch direction, porosity on various types of patterns and dimensions, metal catalysts (e.g., Ag, Pt, Ag, Pd), substrate doping concentrations,<sup>17</sup> acid and oxidants, solution concentration, and temperature have been reported extensively.<sup>18</sup>

Recently, overcoming the detouring tendency of small and discrete catalysts, we have achieved highly uniform submicrometer scale c-Si via array by balancing the CG and MT rates during MacEtch.<sup>16</sup> However, the same MacEtch recipe for c-Si via formation did not yield HAR polycrystalline Si (poly-Si) vertical via arrays where the poly-Si vias twisted randomly while the catalyst dots descended. Efforts to readjust etching condition failed to correct the detouring. We believe the inherent polycrystalline grains and grain boundaries make the CG and MT rates vary as MacEtch proceeds downward, making it difficult to achieve the dynamic balance between CG and MT for uniform vertical etching.

Note that Chang et al. reported the successful fabrication of poly-Si and amorphous Si vertical NW arrays,<sup>19</sup> by confining the etching direction using sparsely spaced mesh patterns. In addition, the fabrication of vertical trenches in c-Si using porous metal catalyst has been also reported by Li et al.<sup>20</sup> and Romano et al.<sup>21</sup> However, their work is limited to interconnected mesh and trench pattern catalysts of particular type of dimensions and does not fully apply when discrete catalysts of submicrometer sizes are required for small via formation in poly-Si.

In this work, we present a universal method, self-anchored catalyst (SAC) MacEtch, to enhance MT and anchor the catalyst while it descends to the body of the semiconductor materials, to produce highly uniform, submicrometer scale poly-Si via array. Figure 1 schematically illustrates the mechanism of SAC-MacEtch. SAC-MacEtch uses a porous metal catalyst film (Figure 1a) that confines the etching direction by forming NWs through the pinholes in the porous catalyst (Figure 1b). As long as the pinholes are small enough, the produced NWs will be trimmed (Figure 1c) automatically during etching from diffused holes away from the Au–Si interface, i.e., remote MacEtch, only leaving the bottom part to anchor the catalyst dot from moving, thus the self-anchoring nature. Here we report the successful demonstration of poly-Si via arrays with diameters varying from 200 to 900 nm at a fixed 1 μm pitch using SAC-MacEtch, proving



**Figure 1.** Schematic illustration of the SAC-MacEtch mechanism for poly-Si: (a) deposition of porous Au film on poly-Si; (b) NWs formed through the pinholes while the porous Au film descended; (c) NWs chemically etched by remote MacEtch to become thinner and shorter; (d) vertical via formation in poly-Si with the NWs self-polished away.

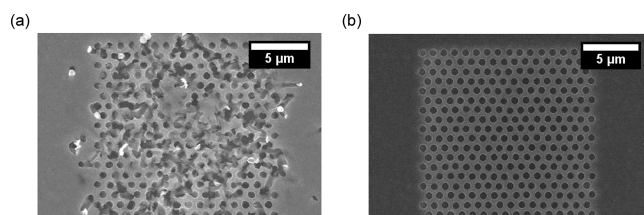
the effectiveness of the anchoring effect. We further demonstrate the formation of vertical via array on multistacked poly-Si/SiO<sub>2</sub> structure by SAC-MacEtch without catalyst delamination or deformation, which can potentially impact the 2.5D/3D photonic and electronic device applications significantly. Finally, we show that SAC-MacEtch can also provide significant mass transport enhancement to enable the formation of TSVs with lateral feature sizes that are on the submillimeter scale.

## RESULTS AND DISCUSSION

Nonporous (continuous) and porous Au catalyst dot arrays, with the dot diameters varying from 200 to 900 nm at 1 μm fixed pitch, were patterned on a poly-Si sample (2 μm thick poly-Si on 100 nm-thick SiO<sub>2</sub> on c-Si) and MacEtched in a solution mixture of HF, H<sub>2</sub>O<sub>2</sub>, IPA, and DI water. The porosity of the catalyst dots is controlled simply through evaporation thickness and rate. Details can be found in Methods. The molar concentration ratio of the HF and H<sub>2</sub>O<sub>2</sub>, as defined in eq 1, varied from 0.1 to 0.32.

$$\rho_{\text{H}_2\text{O}_2} = \frac{\text{H}_2\text{O}_2 \text{ (M)}}{\text{HF (M)} + \text{H}_2\text{O}_2 \text{ (M)}} \quad (1)$$

Figure 2a shows the top view SEM image of the etched morphology using nonporous Au catalyst array of 700 nm diameter



**Figure 2.** Top view SEM images of a 700 nm diameter via array produced using (a) nonporous and (b) porous Au catalyst film, respectively, in a MacEtch solution with  $\rho_{\text{H}_2\text{O}_2} = 0.32$  for 10 min.

dots, MacEtched in 0.32  $\rho_{\text{H}_2\text{O}_2}$  for 10 min. Catalyst detouring normally originates from catalyst motion induced by the trapped H<sub>2</sub> (one of the etching byproducts),<sup>22</sup> limited mass transport,<sup>23</sup> or nonuniform mass transport rate under the catalyst due to the

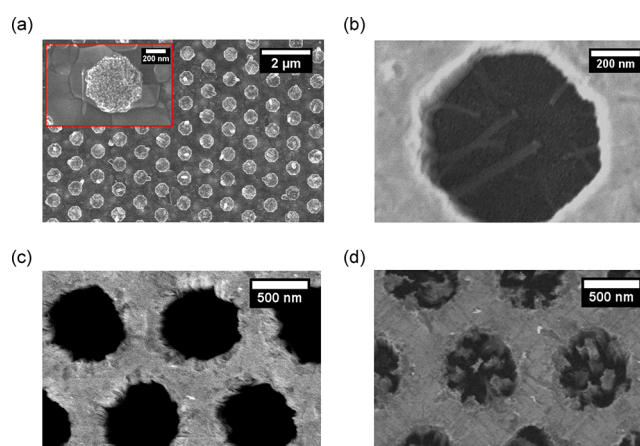
limited liquid access.<sup>24</sup> By decreasing the oxidant concentration (thus reducing H<sub>2</sub> generation), the catalyst delamination was minimized, but the catalyst detour within every etched via could not be avoided (Figure S1 in Supporting Information).

The nonuniform etching under the catalyst becomes more evident as the catalyst diameter decreases. Figure S1a and Figure S1b show the top view SEM images of nonporous Au catalyst array of 200 and 900 nm diameter dots at 1 μm pitch, respectively, MacEtched in 0.1 ρ<sub>H<sub>2</sub>O<sub>2</sub></sub> for 10 min. Inset of Figure S1a shows a zoom-in image of the detoured catalyst. Scale bar is 50 nm. At lower H<sub>2</sub>O<sub>2</sub> concentration, although the catalyst delamination is minimized as expected, the catalyst detouring within every etched via is observed. It can be seen that as the catalyst diameter decreases, catalyst deformation is reduced; however, the catalyst detouring to random directions is increased.

Obviously, the grains in poly-Si contain crystallites with different crystal orientations. The discrete catalyst motion can easily be directed away from the vertical trajectory if the etch rate is uneven spatially as a result of grain size and orientation difference in the polycrystalline structure underneath the catalyst. As reported by Chern et al.<sup>25</sup> in their study of MacEtch using Ag mesh patterned catalyst on (100), (110), (111) c-Si substrates, the etching proceeded preferably in ⟨100⟩ direction at high oxidant concentration, due to the limited amount of HF, and the preferred etching direction changed to ⟨110⟩ and ⟨111⟩ at low oxidant concentration. For polycrystals, when the catalyst overlaps with more than one grain (the grain size varies from ~200 to ~300 nm), the etch rate under the catalyst becomes nonuniform, and the catalyst dots tilt to the direction of the grain where the etch rate is the fastest. It should be noted that etching occurs more readily and faster at the grain boundaries because the grain boundary atoms are more easily and rapidly dissolved than the atoms within the grains.<sup>26</sup> Therefore, both the presence of different crystal orientations and the grain boundaries of poly-Si are attributed to nonuniform etching under the catalyst deposited on poly-Si. We believe this is the reason that prevented continued etching vertically into the poly-Si, when the same etching recipe and same patterning were used to produce perfectly ordered via arrays in c-Si of similar doping levels.

In order to confine the etching direction normal to the substrate continuously, instead of depositing a continuous catalyst film, porous catalyst can be deposited by controlling the metal thickness and deposition rate. Thus, the formation of porous Au film can be achieved at a deposition condition in between that for discrete island morphology and for nonporous film. The average pinhole size and pore coverage as a function of the Au film thickness at fixed deposition rate for this study can be found in Figure S2. The average pinhole size increases as the deposition thickness decreases or the deposition rate increases. Figure 2b shows the top view SEM image of the etch result under all identical conditions as in Figure 2a, except porous Au catalyst was employed. The catalyst delamination, deformation, and detouring resulting from the uneven etch rate under the catalyst are nearly eliminated as compared to the nonporous catalyst.

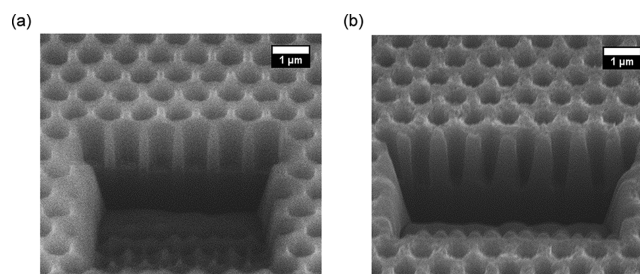
The mechanism of the catalyst anchoring and etch direction confinement in porous catalyst are investigated by examining the resultant samples as a function of etch time. Figure 3a shows the top view SEM image of the porous catalyst array before MacEtch. The inset shows the high magnification image of a single catalyst deposited on the multipoly grains. Figure 3b shows the SEM image of the 700 nm diameter catalyst with porous Au MacEtched in 0.32 ρ<sub>H<sub>2</sub>O<sub>2</sub></sub> for 2 min. NWs of approximately sub-20 nm diameter



**Figure 3.** Top view SEM images of (a) porous catalyst dot (mesh-in-dot) before MacEtch, where inset shows the high magnification view of a single catalyst dot deposited on the multipoly grains; (b) initial stage (2 min) of MacEtch showing the formation of NWs ( $\leq 20$  nm in diameter) through the porous catalyst pinholes; (c) vias showing the NWs are etched after 10 min etching; (d) an example of vias formed by porous catalyst dots with larger ( $\sim 100$  nm) NWs, through bigger pinholes, remaining after 10 min etching.

are formed through the pinholes in the porous Au catalyst film. This makes the catalyst dot similar to the mesh pattern catalyst within the dot area, which is essentially mesh-in-dot double patterning. During the MacEtch, NWs formed through the mesh pinholes anchor (confine) the catalyst dot from delamination and deformation. Figure 3c shows the result after 10 min etching. With the longer etch duration, the NWs are no longer visible from the top, presumably chemically polished away by the diffusion of the unconsumed holes.<sup>27</sup> For comparison, larger NWs ( $\sim 100$  nm, Figure 3d) formed through bigger pinholes in the porous catalyst film remain clearly visible, MacEtched under the same condition as in Figure 3c. This is because only the surface of NWs is chemically etched from the diffusion of the unconsumed holes and it takes longer time for thicker wires to be completely polished away.

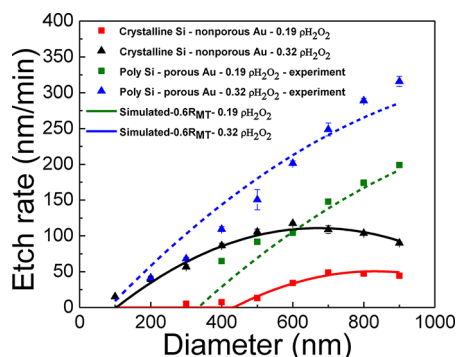
Figure 4a and Figure 4b show the 52°-tilted cross-sectional SEM images of the 800 and 400 nm diameter poly-Si via array



**Figure 4.** 52°-tilted cross-sectional SEM images after FIB showing via array fabricated with porous Au catalyst array of (a) 800 nm and (b) 400 nm diameter, at a fixed pitch of 1 μm, etched in identical MacEtch solution for 10 min.

produced by MacEtch using porous catalyst with sub-20 nm pinholes in 0.32 ρ<sub>H<sub>2</sub>O<sub>2</sub></sub> for 10 min. It can be seen that both 800 and 400 nm diameter catalyst arrays sink down vertically to form poly-Si vias without catalyst detouring or delamination. They also show that the NWs formed through the pinholes are chemically polished away at the end of the etching process.

Next, we systematically examine the SAC-MacEtch rate trend of poly-Si as a function of size and compare with that of c-Si. Shown in Figure 5 is the vertical etch rate as a function of the



**Figure 5.** Plot of measured and simulated etch rates as a function of diameter at a fixed pitch of 1  $\mu\text{m}$ , MacEtched at 0.19 and 0.32  $\rho_{\text{H}_2\text{O}_2}$  for poly (dashed line) and single crystalline (solid lines) Si at conditions indicated.

catalyst diameter at a fixed pitch of 1  $\mu\text{m}$  for c-Si with regular MacEtch and poly-Si with SAC-MacEtch. The symbols, as noted in the figure legend, represent the measured vertical etch rate at the indicated solution concentration, while the solid (black and red) and dashed lines (blue and green) represent the simulated results for c-Si nonporous Au-MacEtch and poly-Si Au SAC-MacEtch, respectively. The corresponding SEM images of the etched structures can be found in the Supporting Information (Figure S3 and S4). Fitting to measured etch rate was performed by the empirical vertical etch rate model.<sup>16</sup>

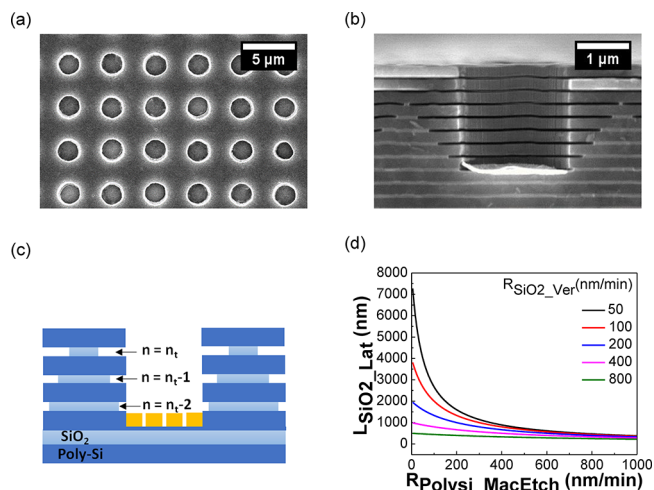
In c-Si (black and red traces), a parabolic dependence of vertical etch rate on via diameter can be seen, consistent with previous reports.<sup>16</sup> This is because the vertical etch rate increases with increasing catalyst diameter due to the enhanced CG (CG rate limited regime), until the diameter reaches a size that is large enough such that MT becomes the rate-determining step, where vertical etch rate decreases with increasing diameter. The etch rate decreases with decreasing  $\text{H}_2\text{O}_2$  concentration, due to the reduced hole injection rate, and the etch rate peak shifts to smaller diameter with increasing oxidant concentration.<sup>16</sup> In contrast, the etch rate in poly-Si SAC-MacEtch continues to increase with diameter (e.g., from 40 to 320 nm/min as the diameter increases from 200 to 900 nm at 0.32  $\rho_{\text{H}_2\text{O}_2}$ ). No saturation or pivoting downward in the same range of diameters as that for the single crystal counterpart is observed. MT process refers to the transport of reactants to and byproducts away from the etching front. Therefore, MT is determined by the size, thickness, morphology of the catalyst, and the property of the underlying semiconductors.<sup>28</sup> According to the Lai et al., van der Waals force is one of the primary forces that govern the MT of the reactant and byproducts.<sup>29</sup> The change in MT by the difference in van der Waals force between the single crystalline vs polycrystalline structures should not be significant as compared to the one between the different materials (e.g., Si vs GaAs). We therefore attribute most of the MT enhancement to the porous catalyst, which enables additional etchant solution access through the pinholes. The amount of MT enhancement can be estimated by fitting the experimental etch rate data to empirical vertical etch rate model<sup>16</sup> as described as

$$R_{\text{MacEtch}} = a + xR_{\text{MT}} + R_{\text{CG}} \quad (2)$$

where  $a$  is the intercept,  $R_{\text{CG}}$  is the etch rate increased by the CG, and  $R_{\text{MT}}$  is the etch rate decrease by the limited MT.  $R_{\text{MT}} = -bD - cD^2$  and  $R_{\text{CG}} = bP - cP^2 + 2cDP$ , where  $D$  and  $P$  are the diameter and pitch of the catalyst array and  $b$  and  $c$  are extracted first and second order polynomial coefficients. Extracted values of the parameters of  $a$ ,  $b$ , and  $c$  are 40.78, 108.71, and 320.72 for 0.19  $\rho_{\text{H}_2\text{O}_2}$  and 74.08, 214.98, and 319.58 for 0.32  $\rho_{\text{H}_2\text{O}_2}$ . The detailed derivation of the empirical etch rate model can be found in the work by Kim et al.<sup>16</sup>

For simplicity, the decrease in CG with porous catalyst vs continuous catalyst film can be treated as negligible because of the small pore size; and under the oxidant concentration range studied here, we can assume the difference in net etch rate of poly-Si and c-Si without grain boundary consideration is small because of the weak dependence on crystal orientation.<sup>18</sup> Then the etch rate of the poly-Si can be fitted by replacing the  $R_{\text{MT}}$  with  $xR_{\text{MT}}$ , which indicates that the etch rate decreased by MT ( $R_{\text{MT}}$ ) is reduced by  $x$  percent. The poly-Si etch rates for both 0.19 and 0.32  $\rho_{\text{H}_2\text{O}_2}$  fit when  $x = 0.6$ , which indicates that the vertical etch rate decreased by the limited MT is reduced by 60% (i.e., MT is enhanced by 40%). This confirms the enhanced mass transport nature of SAC-MacEtch, in addition to its anchoring effect.

With use of the SAC-MacEtch, not only the motion of the catalyst can be confined, but also the MT can be engineered to fabricate the complex 3D via array structures. Figure 6a and



**Figure 6.** (a) Top and (b) cross-sectional SEM images of 2  $\mu\text{m}$  diameter and 4  $\mu\text{m}$  pitch via array formed on poly-Si/SiO<sub>2</sub> stacks by MacEtched at 0.32  $\rho_{\text{H}_2\text{O}_2}$  for 5 min, (c) cross-sectional schematic of the etched via with SiO<sub>2</sub> lateral etching, (d) simulated SiO<sub>2</sub> lateral etching depth ( $L_{\text{SiO}_2\text{Lat}}(n)$ ) as a function of poly-Si MacEtch rate ( $R_{\text{Polys\_MacEtch}}$ ) at varied SiO<sub>2</sub> vertical etch rate ( $R_{\text{SiO}_2\text{Ver}}$ ).

Figure 6b show top and cross-sectional SEM images of 2  $\mu\text{m}$  diameter discrete dot catalyst array at pitch of 4  $\mu\text{m}$  deposited on the 200/50 nm poly-Si/SiO<sub>2</sub> stacked substrate, MacEtched in 0.32  $\rho_{\text{H}_2\text{O}_2}$  for 5 min. The catalyst vertically etches through the poly-Si by SAC-MacEtch, then continues to etch through the SiO<sub>2</sub> layer by chemical etching. During this etching process, the catalyst is anchored from delamination and detouring such that it forms the uniform through via array on the stacked poly-Si/SiO<sub>2</sub> substrate. Note that the SiO<sub>2</sub> layers are laterally etched; etch depth linearly increases from 256 to 910 nm from the bottom to the top of the SiO<sub>2</sub> layers. The SiO<sub>2</sub> lateral etching starts when the SiO<sub>2</sub> layer is exposed right after catalyst etches through the poly-Si

placed above the SiO<sub>2</sub> layer such that the time that SiO<sub>2</sub> layer is exposed to solution for lateral etching decreases for the deeper layer.

The lateral etch depth of the first SiO<sub>2</sub> layer is smaller than the vertical via etch depth. This indicates that the lateral etch rate of the SiO<sub>2</sub> is slower than the vertical etch rate of poly-Si and SiO<sub>2</sub>. The MT of the poly-Si and the SiO<sub>2</sub> vertical etching is greater than the MT of SiO<sub>2</sub> lateral etching; MT of the vertical etching is enhanced by the porous catalyst, while the MT of the SiO<sub>2</sub> lateral etching is limited by the thickness of the SiO<sub>2</sub>.

Figure 6c shows the cross-sectional schematic of the etched poly-Si/SiO<sub>2</sub> stacked via. The lateral etch depth for the *n*th SiO<sub>2</sub> layer ( $L_{\text{SiO}_2\text{-Lat}}(n)$ ) can be analytically described as

$$L_{\text{SiO}_2\text{-Lat}}(n) = R_{\text{SiO}_2\text{-Lat}} \times \frac{n}{n_t} \quad (3)$$

where  $n_t$  is the total number of the stacked poly-Si/SiO<sub>2</sub> vertically etched through,  $R_{\text{SiO}_2\text{-Lat}}$  is the SiO<sub>2</sub> lateral etch rate, and  $t$  is the total etch time.

On the other hand, the vertical etch depth through stacked poly-Si/SiO<sub>2</sub> can be described as

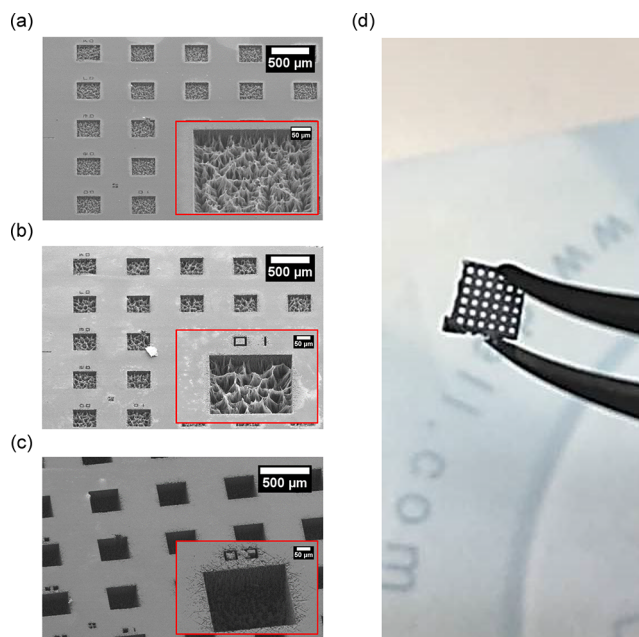
$$L_{\text{Ver}} = (R_{\text{Polysil-MacEtch}} + R_{\text{SiO}_2\text{-Ver}}) \times t \quad (4)$$

where  $L_{\text{Ver}}$  is the vertical etch depth,  $R_{\text{Polysil-MacEtch}}$  is the poly-Si vertical MacEtch rate,  $R_{\text{SiO}_2\text{-Ver}}$  is the SiO<sub>2</sub> vertical etch rate.  $R_{\text{SiO}_2\text{-Lat}}$  and  $R_{\text{SiO}_2\text{-Ver}}$  are different due to the etch rate difference from the limited MT. Since the  $t$  is the same, eqs 3 and 4 can be combined as

$$L_{\text{SiO}_2\text{-Lat}}(n) = \frac{n(R_{\text{SiO}_2\text{-Lat}} \times L_{\text{Ver}})}{n_t(R_{\text{Polysil-MacEtch}} + R_{\text{SiO}_2\text{-Ver}})} \quad (5)$$

This indicates that the  $L_{\text{SiO}_2\text{-Lat}}(n)$  can be quenched by increasing the  $R_{\text{Polysil-MacEtch}}$  or  $R_{\text{SiO}_2\text{-Ver}}$  or decreasing the  $R_{\text{SiO}_2\text{-Lat}}$ .  $R_{\text{Polysil-MacEtch}}$  can be increased by increasing H<sub>2</sub>O<sub>2</sub> concentration,  $R_{\text{SiO}_2\text{-Ver}}$  can be increased by increasing the catalyst pinhole density. Note that  $R_{\text{SiO}_2\text{-Ver}}$  and  $R_{\text{SiO}_2\text{-Lat}}$  are simultaneously affected by the solution concentration. Figure 6d shows the simulated  $L_{\text{SiO}_2\text{-Lat}}(n = n_t)$  as a function of  $R_{\text{Polysil-MacEtch}}$  from 5 to 1000 nm/min at various  $R_{\text{SiO}_2\text{-Ver}}$  from 50 to 800 nm/min. The  $L_{\text{Ver}}$  is fixed to 2 μm,  $R_{\text{SiO}_2\text{-Lat}}$  is fixed to 200 nm/min.  $L_{\text{SiO}_2\text{-Lat}}$  decreases as the  $R_{\text{Polysil-MacEtch}}$  increases and then gets saturated at large  $R_{\text{Polysil-MacEtch}}$ .  $L_{\text{SiO}_2\text{-Lat}}$  decreases as the  $R_{\text{SiO}_2\text{-Ver}}$  increases from 50 to 800 nm/min. The decrease in  $L_{\text{SiO}_2\text{-Lat}}$  with increasing  $R_{\text{SiO}_2\text{-Ver}}$  is larger for low  $R_{\text{Polysil-MacEtch}}$ .

Clearly, SAC-MacEtch plays a critical role in enhancing mass transport and preventing the catalyst movement due to uneven etching in polycrystals. This technique can be equally powerful for single crystal etching where the liquid access is restricted. For example, the fabrication of via arrays over a 4-in. wafer with via diameter of 27.1–29.7 μm and depth of 159–164 μm in c-Si using porous metal catalyst has been reported by Li et al.<sup>30</sup> Shown in Figure 7 are SEM and optical images showing the process of achieving silicon vias as wide as 320 μm all the way through on a piece of 550 μm thick wafer using SAC-MacEtch at 0.26 ρ<sub>H<sub>2</sub>O<sub>2</sub></sub>. While NWs were formed and clumped together inside the vias after 1.5 h (Figure 7a) and 6 h (Figure 7b) of MacEtch, most of NWs were chemically etched after 48 h (Figure 7c). Porous catalyst film continued to descend into the c-Si wafer, enabling a complete formation of TSV in 550 μm thick



**Figure 7.** 45°-tilted SEM images of 320 × 320 μm<sup>2</sup> via array in single crystal Si fabricated with porous Au catalysts as a function of etching time ((a) 1.5 h, (b) 6 h, and (c) 48 h), under MacEtch in 0.26 ρ<sub>H<sub>2</sub>O<sub>2</sub></sub>. (d) Optical image of a TSV array in a piece of single crystal 550 μm thick Si wafer after 96 h of etching.

c-Si after 96 h (Figure 7d) of MacEtch. The lateral dimension and vertical depth of our TSVs are nearly half a millimeter, which are extremely challenging scales unprecedented for MacEtch to tackle. SAC-MacEtch exactly fulfilled the needs to meet both challenges. It should be noted that sidewall roughness and porosity of these TSVs are not well-controlled due to the extended time required at the specified condition to allow the etching through the entire wafer thickness. The sidewall morphology of the TSV can be optimized by speeding up the etching via magnetic-field-guided MacEtch<sup>31</sup> or dual patterning of porous catalyst on both front and backside of the substrate with precise alignment.

## CONCLUSION

We have developed and demonstrated the effectiveness of the SAC-MacEtch on via formation in poly-Si and poly-Si/SiO<sub>2</sub> stack. Uniform vertical etching has been achieved by balancing CG and MT despite the randomly distributed polycrystalline grains and grain boundaries. Vertical MacEtch rate of poly-Si using porous catalyst arrays was systemically studied by varying catalyst dot diameter at fixed 1 μm pitch. Under 1 μm pitch, etching rate increased continuously as the diameter increased up to 900 nm, without saturation in etching rate, which is attributed mostly to the enhanced MT by solution access through the pinholes in the porous catalyst. Subsequently, an array of vias with diameters of 2 μm at a fixed pitch of 4 μm has been realized on poly-Si/SiO<sub>2</sub> stacks through poly-Si SAC-MacEtch and SiO<sub>2</sub> chemical etching. Also, for the first time, enabled by the anchoring effect and enhanced etchant access through the porous catalyst in SAC-MacEtch, submillimeter lateral scale TSVs through the entire depth of a wafer (550 μm) are realized with excellent site specificity in c-Si. This study shows that the SAC-MacEtch plays a critical role in achieving closely packed submicrometer size vias in poly-Si potentially not only for high density memory and optoelectronic device applications but also for large TSVs interconnect in 3D integrated circuits. On the fundamental side,

SAC-MacEtch reveals that the onset of the mass-transport limited critical diameter is delayed significantly compared to the nonporous catalyst c-Si counterpart and confirms the interplay of the CG and MT fundamental aspects in the MacEtch mechanism.<sup>32</sup>

## METHODS

**SAC-MacEtch on Poly-Si.** The substrate consists of 2  $\mu\text{m}$  low-pressure chemical vapor deposition (LPCVD) grown poly-Si on oxide deposited on boron doped p-type (100)-oriented c-Si with resistivity of 1–50  $\Omega\text{-cm}$ . Prior to any process, the substrate was subjected to a RCA cleaning processes: organic contaminants removal in 1:1:5 ammonium hydroxide ( $\text{NH}_4\text{OH}$ )/hydrogen peroxide ( $\text{H}_2\text{O}_2$ )/deionized water (DI) at 80  $^\circ\text{C}$ , native oxide stripe in 1:10 buffer oxide etchant (BOE) and ionic contaminant removal in 1:1 hydrogen chloride (HCl)/DI. After the cleaning process, electron lithography resist of 950 poly(methyl methacrylate) (PMMA) in 2% anisole was spin coated at 2500 rpm for 30 s to deposit 80 nm resist film on the substrate. Then electron beam lithography with 10 kV beam voltage and 20  $\mu\text{m}$  aperture was used for exposure of submicrometer dot array patterns. The exposed patterns were developed in 1:3 methyl isobutyl ketone (MIBK)/isopropyl alcohol (IPA) for 2 min at room temperature. Then porous (6 nm thick) Au and nonporous (18 nm thick) Au were deposited at deposition rate of 0.7  $\text{\AA}/\text{s}$  using CHA SEC-600 electron beam evaporator for the MacEtch comparison. Subsequently, the deposited Au film on the PMMA was lifted off by immersing the samples in remover PG for 30 min at 60  $^\circ\text{C}$  and sonicating in the IPA for 10 min.

Both samples with porous and nonporous Au were MacEtched in the solution of 49% hydrofluoric acid (HF, 0.56 M), 30% hydrogen peroxide ( $\text{H}_2\text{O}_2$ , 0.13 M, 0.26 M), isopropyl alcohol (IPA, 0.21 M), and DI (0.88 M). The top view of the etched samples was inspected with a Hitachi S-4800 scanning electron microscope (SEM), and the cross section of the etched samples was inspected with FEI DB 235 dual-beam focused ion beam (FIB) system.

**SAC-MacEtch on Poly-Si/SiO<sub>2</sub> Stack.** The substrate consists of 20 pairs of LPCVD grown 200 nm poly-Si and 50 nm SiO<sub>2</sub> stack on boron doped p-type (100)-oriented c-Si. Prior to any process, the substrate was thoroughly cleaned by the same cleaning method as described above. Micrometer scale via array with a diameter of 2  $\mu\text{m}$  at a fixed 4  $\mu\text{m}$  pitch was patterned on the substrate using a standard photolithography. Then the porous Au was deposited with a deposition rate of 0.7  $\text{\AA}/\text{s}$  by CHA electron beam evaporator. The sample was MacEtched in a solution of 49% hydrofluoric acid (HF, 0.56 M), 30% hydrogen peroxide ( $\text{H}_2\text{O}_2$ , 0.26 M), isopropyl alcohol (IPA, 0.21 M), and DI (0.88 M) for 5 min.

**SAC-MacEtch on c-Si for TSV.** The substrate is a 550  $\mu\text{m}$  thick p-type (100)-oriented c-Si with resistivity of 1–50  $\Omega\text{-cm}$ . Submillimeter scale square via array with a size of 320  $\times$  320  $\mu\text{m}^2$  was patterned by the standard photolithography. Then porous Au was deposited with a deposition rate of 0.7  $\text{\AA}/\text{s}$  by CHA electron beam evaporator. The sample was MacEtched in a solution of 49% hydrofluoric acid (HF, 0.56 M), 30% hydrogen peroxide ( $\text{H}_2\text{O}_2$ , 0.26 M), isopropyl alcohol (IPA, 0.21 M), and DI (0.88 M) for 1.5, 6, 48, and 96 h, respectively. The MacEtch solution was replaced every 3 h to prevent the change in solution concentration due to the solution evaporation and consumption.

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b17708.

SEM images and pore size and coverage (PDF)

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### Notes

The authors declare no competing financial interest.

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