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High-Speed Planar GaAs Nanowire Arrays with f_{max} > 75 GHz by Wafer-Scale Bottom-up Growth

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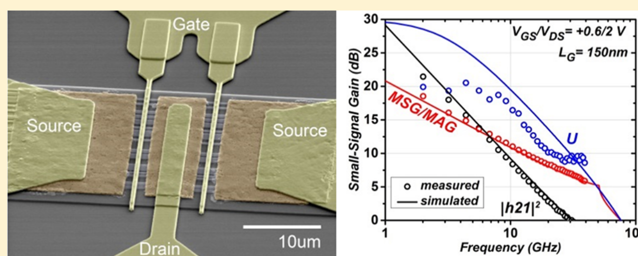
Supporting Information

ABSTRACT: Wafer-scale defect-free planar III−V nanowire (NW) arrays with ∼100% yield and precisely defined positions are realized via a patterned vapor−liquid−solid (VLS) growth method. Long and uniform planar GaAs NWs were assembled in perfectly parallel arrays to form double-channel T-gated NW array-based high electron mobility transistors (HEMTs) with DC and RF performance surpassing those for all field-effect transistors (FETs) with VLS NWs, carbon nanotubes (CNTs), or graphene channels in-plane with the substrate. For a planar GaAs NW array-based HEMT with 150 nm gate length and 2 V drain bias, the on/off ratio (I_{ON}/I_{OFF}), cutoff frequency (f_T), and maximum oscillation frequency (f_{max}) are 10^4, 33, and 75 GHz, respectively. By characterizing more than 100 devices on a 1.5 × 1.5 cm^2 chip, we prove chip-level electrical uniformity of the planar NW array-based HEMTs and verify the feasibility of using this bottom-up planar NW technology for post-Si large-scale nanoelectronics.



KEYWORDS: *Bottom-up, VLS, nanowire, III−V, transistor, VLSI*

To increase transistor density and improve circuit performance, the semiconductor chip industry has been driven to constantly scale down critical feature sizes in transistors. As the scaling continues, severe short channel effects (SCE) forfeit performance gains via pure dimensional down-scaling.[1] New transistor architectures and materials are needed to boost the performance with further down-scaling.[1,2] Si-based trigate and ultrathin-body transistors have demonstrated superior electrostatics and enhanced carrier mobility compared to traditional bulk Si technology.[3,4] III−V nanowires (NWs), carbon nanotubes (CNTs), and graphene are under extensive research for possible uses in post-Si transistor technology because they all have inherent three-dimensional (3D) or ultrathin structures for SCE control and possess much greater carrier mobility than Si.[2,5−7] Good electrostatics and high carrier mobility are also beneficial for the intrinsic gain (G_m/G_{ds}, where G_m is the transconductance and G_{ds} is the output conductance),[8] enabling analog/RF features for system-on-chip (SOC) applications.[4,9] Although some CNTs have finite band gaps, synthesizing 100% semiconductor CNTs with uniform diameters and placing them precisely in high density on a wafer has proven difficult for large-scale integrated circuit (IC) applications.[6] Alternatively, the synthesis of wafer-scale single-crystal monolayer graphene seems feasible for large-scale applications, but digital ICs cannot be built on graphene due to its metal-like band structure.[7,10] In contrast, III−V NWs have well-defined and tunable bandgaps (via composition modulation), and can be fabricated in large-scale with precise site-control.[2,5] Therefore, III−V NWs are the most promising candidates for post-Si SOC applications.

Vertical III−V NW field-effect transistors (FETs) have been demonstrated with site-controlled III−V NW channels defined by top-down dry etching,[11] selective area epitaxy (SAE),[12] and vapor−liquid−solid (VLS) bottom-up methods.[13−15] However, the vertical device layout makes vertical NW FETs incompatible with mainstream planar processing. Vertical NW FETs also have more issues with parasitic resistance and capacitance compared to planar NW FETs. Thus, planar NW FETs are preferable for high-performance digital and RF applications. There have been many studies on planar III−V NW FETs fabricated through the top-down dry etching approach.[16−19] The top-down approach requires complex patterning techniques and introduces damage and defects in the NWs. Bottom-up III−V NWs are made from constructive methods and are supposed to have much better material quality.[20] However, the SAE method has an even higher level of processing complexity comparing with the top-down dry etching approach.[21] The

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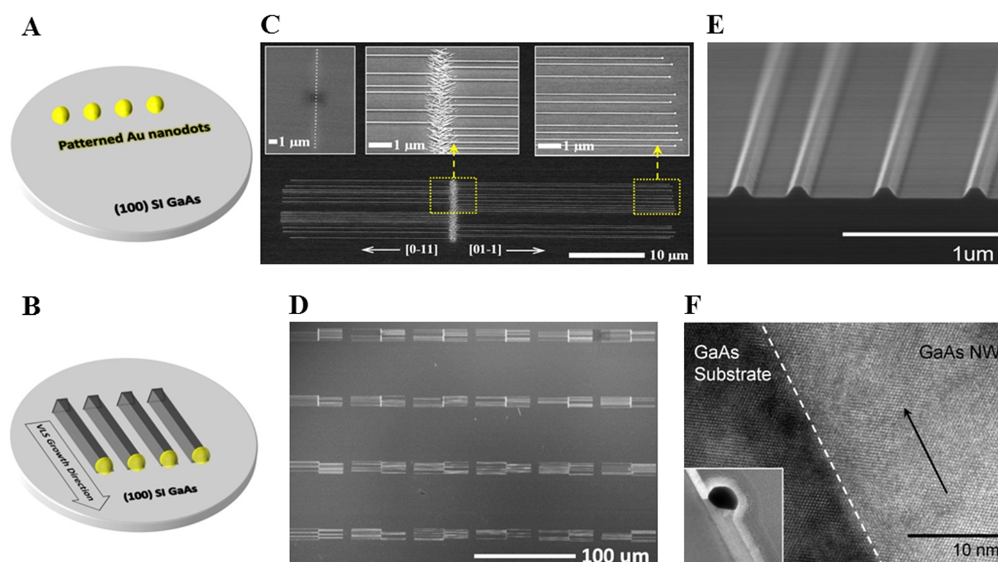

Figure 1. Planar GaAs NW arrays. (A) Au seeds are formed by EBL, Au evaporation, and lift-off processes. (B) VLS growth of planar GaAs NWs in parallel arrays on SI GaAs substrates. (C) Tilt-view SEM image of a representative planar GaAs NW array with 100% planar NW yield. The planar NWs grow bidirectionally in the antiparallel $[0\bar{1}1]$ and $[01\bar{1}]$ directions. Insets, from the left to the right, show the patterned Au seeds, the dividing line between the oppositely propagated NWs and the near-tip portions of the $[01\bar{1}]$ planar NWs. (D) Top-view SEM image of 4 × 6 planar GaAs NW arrays, illustrating the wafer-scale growth capability. (E) Tilt-view SEM image of a cleaved planar GaAs NW array. The planar NWs have perfectly uniform trapezoidal cross sections. (F) HR-TEM image of a representative planar GaAs NW liberated from the as-grown sample (the black arrow indicates the NW growth direction), showing its defect-free and zinc-blende construction. The inset highlights the cross-sectional geometry of the Au nanoparticle relative to the NW and substrate.

morphologies of SAE planar III−V NWs have strong dependence on the top-down patterning profiles of the SAE templates, which can lead to nonuniform SAE NWs. VLS III−V NWs grown from patterned Au seeds require much less patterning efforts (requiring a dot pattern instead of a line) and prove to have very uniform morphologies.[5] Because the sizes of VLS III−V NWs are determined by the volumes of the Au seeds, VLS NWs can have feature sizes smaller than what the patterning can offer. Given the fact that VLS III−V NWs prefer to grow in the ⟨111⟩B directions,[22] only VLS vertical III−V NW arrays have been demonstrated using III−V (111)B substrates.[13−15] In order to make planar NW FETs, many postgrowth alignment methods have been developed to align the as-grown vertical III−V NWs in-plane with the substrates such as contact printing,[23] field-assisted,[24] blown bubble,[25] combing,[26] sliding,[27] Langmuir−Blodgett,[28] microfluidics,[29,30] or dielectrophoresis.[31,32] Aside from the additional processing complexity involved in these alignment processes, none of them have the precise NW positioning capability required for making large-scale ICs. So far, the best planar III−V NW FETs fabricated by aligning VLS vertical InAs NWs in-plane with the substrates report f_{max} = 1.8 GHz, which is far less than its high mobility would predict.[33]

VLS planar NWs have an epitaxial relation with the host substrates and are fully compatible with mainstream planar processing.[34] Our group first reported the controlled VLS growth of ⟨110⟩ planar GaAs NWs on semi-insulating (SI) (100) GaAs substrates using randomly dispersed Au colloids as the growth seeds.[34] Using this growth method, planar GaAs NW metal−semiconductor FETs (MESFETs), high electron mobility transistors (HEMTs), and metal−oxide−semiconductor FETs (MOSFETs) were demonstrated with good DC characteristics.[20,35−38] However, the random distribution of the dispersed Au colloids prevents the realization of large-scale ICs using these planar GaAs NW FETs. Growing from top-down patterned Au seeds, VLS planar ZnO NW arrays on R-plane sapphire substrates were achieved.[39] However, due to the nonideal NW quality, the performance of the FETs made from the ZnO NW arrays is far below what is needed for post-Si ICs. Similar work using ZnO VLS NW arrays on *c*-plane GaN and GaN on (0001) sapphire was also demonstrated with more than two crystallographic directions, which makes parallel arrays challenging.[40,41]

In this paper, we report a major milestone to realize wafer-scale defect-free VLS planar III−V NW arrays with ~100% yield and precisely defined positions. For the first time, planar NW array-based HEMTs are demonstrated with record-breaking DC and RF performances among planar FETs with VLS NWs, CNTs, or graphene channels. This work verifies the feasibility of using our bottom-up planar NW technology for post-Si large-scale nanoelectronics and brings the bottom-up nanotechnology a large step forward toward real-world applications.

Growth of Planar NW Arrays. The growth of wafer-scale planar GaAs NW arrays, as illustrated in Figure 1A,B, begins by patterning arrays of Au seeds. Arrays of Au seeds (disk-shape) with diameters of 50 to 300 nm, center-to-center pitch of 100 to 500 nm and a uniform height of 50 nm were formed on SI (100) GaAs substrates via electron beam lithography (EBL), Au evaporation and lift-off processes. The feature sizes of the NWs can be smaller than the EBL pattern sizes if a thin enough Au evaporation is used because the volume of the Au seed determines the NW size. Because VLS planar NWs have an epitaxial relation with the substrates, stringent sample cleaning procedures were applied after Au seed deposition and before the VLS growth to ensure high planar NW yield. The VLS NW growth was carried out in an Aixtron 200/4 metal−organic chemical vapor deposition (MOCVD) reactor using a two-temperature-step (450 → 435 °C) growth method (see Methods).[37] Figure 1C shows a tilt-view scanning electron

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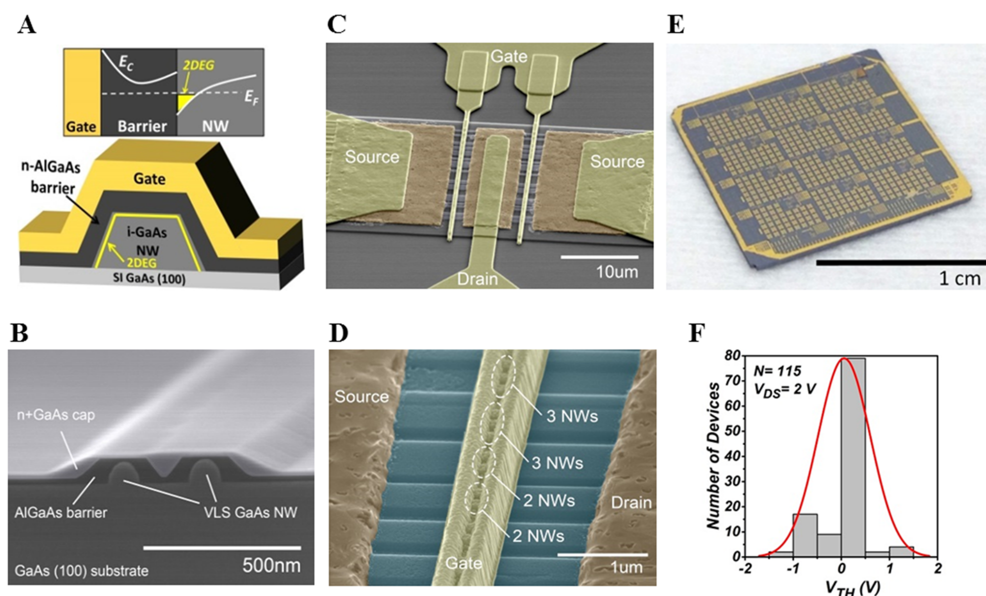

Figure 2. Planar NW array-based HEMTs. (A) Illustration of the operation mechanism of planar NW array-based HEMTs. (B) Cross-section of the planar NW heterostructure with two identical GaAs NWs sharing the $Al_{0.33}Ga_{0.67}As$ barrier. (C) Tilt-view false-color SEM image of a representative fully fabricated planar NW array-based HEMT with L_G = 150 nm and 30 planar GaAs NWs spanning across both channels. (D) Magnified false-color SEM image of the device's (shown in C) channel region. (E) Optical image of a fully fabricated 1.5 × 1.5 cm^2 device chip with 115 precisely positioned planar NW array-based HEMTs. (F) Histogram and Gaussian distribution of the 115 devices and threshold voltage extrapolated by a tangent line from I_{DS} at peak transconductance condition to I_{DS} = 0 V at V_{DS} = 2 V.

microscope (SEM) image of a representative planar GaAs NW array with 100% planar NW yield. The planar GaAs NWs grow bidirectionally in the antiparallel $[0\bar{1}1]$ and $[01\bar{1}]$ directions, with respective lengths of ~22 and 28 μm for the 140 s growth. The origin of the difference in growth rate for the two presumably crystallographically equivalent directions is under further study. Because of the bidirectionality, the grown NWs are no longer equally spaced; wherever there are missing NWs in the array propagating to one side, they can be surely found on the other side. The insets of Figure 1C, from the left to the right, show the patterned Au seeds, the dividing line between the oppositely propagated NWs and the near-tip portions of the $[01\bar{1}]$ planar NWs. The tiny out-of-plane GaAs whiskers at the dividing line are originated from tiny Au particles split from the patterned Au seeds. Figure 1D is the top-view SEM image of 4 × 6 planar GaAs NW arrays on the same sample illustrating the wafer-scale growth capability. The probabilities of planar GaAs nanowires growing in the $[0\bar{1}1]$ and $[01\bar{1}]$ directions are about equal because the $[0\bar{1}1]$ and $[01\bar{1}]$ directions are crystallographically equivalent.[42] The tilt-view SEM image of a cleaved planar GaAs NW array in Figure 1E shows that the planar GaAs NWs grown from the patterned seeds have perfectly uniform trapezoidal cross sections. High-resolution transmission electron micrograph (HR-TEM) analysis (see Supporting Information) of a representative planar NW liberated from the as-grown sample reveals a purely zinc-blende NW crystal structure, entirely free of twin-defects and stacking faults, with VLS growth along the ⟨110⟩ direction. Figure 1F shows the HR-TEM image of the planar NW and substrate interface (the black arrow indicates the NW growth direction). The inset shows a reduced magnification image that highlights the cross-sectional geometry of the Au nanoparticle (dark contrast) relative to the NW and substrate.

Growth and Fabrication of Planar NW Array-Based HEMTs. To explore the electronic properties of the planar NW arrays, a 1.5 × 1.5 cm^2 device chip with 115 planar NW array-based HEMTs in repeating reticles was fabricated for DC/RF characterization. The 115 planar NW array-based HEMTs have various gate lengths and device widths. Au seed arrays were first formed on the SI (100) GaAs substrate in accordance with the mask layout design. Bidirectional ⟨110⟩ planar GaAs NW arrays were then grown for 200 s using the same growth conditions as mentioned above. Upon the cessation of the VLS NW growth, the reactor temperature was raised to 680 °C and pressure was lowered to 100 mbar to grow in situ conformal epitaxial layers comprised of a 3 nm undoped $Al_{0.33}Ga_{0.67}As$ spacer, a 50 nm Si-doped (3 × 10^{18} cm^{-3}) $Al_{0.33}Ga_{0.67}As$ barrier layer, and a 50 nm n^+ (5 × 10^{18} cm^{-3}) GaAs ohmic contact layer. As illustrated in Figure 2A, the operation of a planar NW array-based HEMT relies on the gate's modulation of the two-dimensional electron gas (2DEG) formed at the heterointerfaces between the AlGaAs barrier and the GaAs NW sidewall and top facets.[35] Therefore, a conformal $Al_{0.33}Ga_{0.67}As$ barrier wrapping over the NWs is critical for good device performance. High background H_2 flow was adopted during the barrier growth, which effectively reduced the $Al_{0.33}Ga_{0.67}As$ growth rate and promoted better barrier coating. Figure 2B shows the cross-section of the planar NW heterostructure with two identical GaAs NWs sharing the $Al_{0.33}Ga_{0.67}As$ barrier. Because the growth substrate is semi-insulating, no conduction occurs at the heterointerfaces between the $Al_{0.33}Ga_{0.67}As$ and the GaAs substrate. This was confirmed by characterizing a control device with no NW in the channel (see Supporting Information).

The device fabrication is fully compatible with the planar processing (see Methods). The NWs can be aligned to the mask sets with combinations of EBL and optical lithography. Between the bidirectional planar NW arrays, the relatively longer $[01\bar{1}]$ arrays (~35 μm) were chosen for device processing. Because the $[0\bar{1}1]$ and $[01\bar{1}]$ planar NWs have the same sizes, crystal quality (defect-free), and NW sidewall

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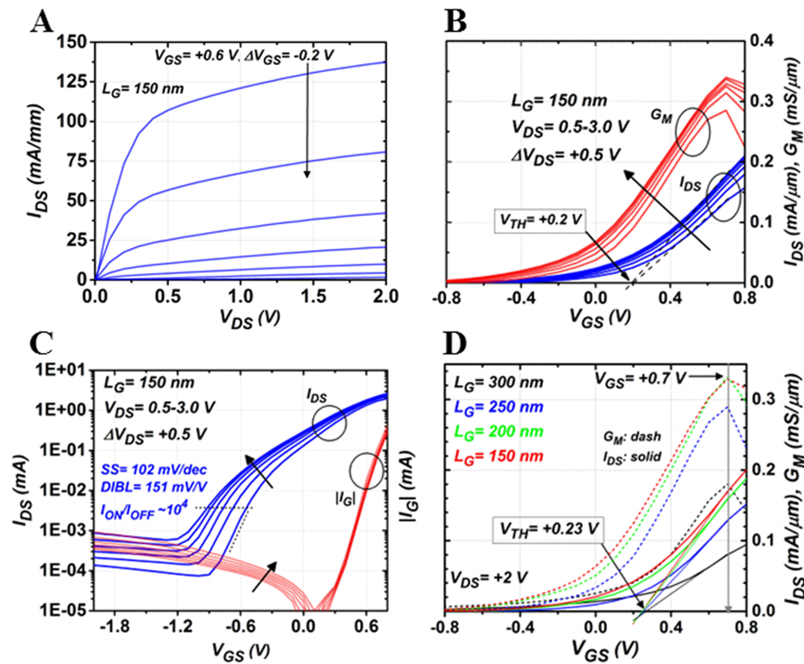

Figure 3. DC characteristics of planar NW array-based HEMTs. (A) Output current versus drain voltage. (B) Transfer characteristics as a function of gate and drain voltage. (C) Log gate and drain current versus gate and drain voltage. (D) Extraction of threshold voltage for the four fabricated gate lengths.

and top facets, they have the same electrical properties.[35] The long $[01\bar{1}]$ planar NW arrays allowed the use of a two-finger T-gated RF pad layout where both gates share the same NWs. A representative fully fabricated device with L_G = 150 nm and 30 planar GaAs NWs spanning across both channels is shown in Figure 2C. Figure 2D is a magnification of the channel region showing all three transistor terminals. It should be noted that NWs in the ungated regions in Figure 2D appear merged. This is because the shared thick n^+ GaAs cap layer buries the original corrugated NWs, as is illustrated in Figure 2B. However, the actual number of NWs can be specified in the center of the T-gate where the n^+ GaAs cap is wet-etched down to the $Al_{0.33}Ga_{0.67}As$ barrier layer. Figure 2E shows the fully fabricated device chip with 115 precisely positioned planar NW array-based HEMTs. Owing to the excellent structural uniformity, the NW HEMTs have excellent electrical uniformity. For example, the histogram (Figure 2F) showing the extracted threshold voltage (V_{TH}) at V_{DS} = 2 V illustrates good distribution centered at the designed V_{TH} (~0 V). By using optimized gate recess etching, even better electrical uniformity can be achieved.

Electrical Characterization and Discussion. The DC current–voltage (I–V) characteristics of a two-finger planar NW array-based HEMT with L_G = 150 nm (as shown in Figure 2C) are plotted in Figure 3A–C. Normalized results are based on the top and two-sidewall NW periphery under the T-gate (W_{NW} = 75 + 75 + 60 = 210 nm). Because there are 30 NWs spanning across both channels, the total device width is 12.6 μm (2 × 30 × 0.21 μm). The output I–V performance shows excellent saturation at low-bias where a maximum transconductance ($G_{m,max}$) is achieved (Figure 3A). Shown in the transfer characteristics (Figure 3B), the V_{TH} was extracted by a tangent I_{DS} line at $G_{m,max}$ and extrapolated to I_{DS} = 0, which is approximately +0.2 V, indicating enhancement mode operation. In Figure 3C, subthreshold slope, SS = 102 mV/dec, and drain-induced barrier lowering, DIBL = 151 mV/V, were extracted along with on/off ratio (I_{ON}/I_{OFF}) ~10^4. In Figure 3D, the linear transfer performance over four studied gate lengths indicates a uniform $G_{m,max}$ gate bias and V_{TH} = +0.23 V, which can be interpreted as negligible SCE in this L_G range.

Small-signal RF performance was characterized in the 0.1–40 GHz range for each L_G shown in Figure 3D. The best de-embedded frequency performance, f_T/f_{max} ~33/75 GHz, was obtained with L_G = 150 nm measured at V_{DS} = 2 V with 30 NWs spreading along a 20 μm contact width—a NW density of ~1.5 NWs/μm (see Supporting Information). To our knowledge, this is the highest reported f_{max} achieved on any nanoscale device with VLS NWs, CNTs, or 2D sheets aligned in-plane with the substrate.[7,33,43−45] Representative gain versus frequency RF measurements are shown in Figure 4A for L_G = 150 nm and V_{GS}/V_{DS} = +0.6/2.0 V. The short-circuit current gain (H_{21}) decreases by −20 dB/dec and falls to 0 dB at f_T = 33 GHz. The maximum available gain (MAG) and unilateral gain (U) are both plotted and extracted to f_{max}= 75 GHz using a conventional small-signal circuit model (see Supporting Information). As expected, the power gains (MAG, U) are well above H_{21} which is indicative of the excellent electrostatics. In Figure 4B,C, the f_T and f_{max} at L_G = 150 nm are mapped for various gate and drain bias, respectively. The peak f_T occurs at lower drain voltage where $G_{m,max}$ is reached without introducing hot-electron effects. The peak f_{max} performance shifts slightly toward high V_{DS} because of its higher sensitivity to gate-to-drain capacitance. In addition, G_m from the 3D NW channel remains high once V_{DS} saturates (~1 V); therefore, a high f_T/f_{max} ~37/67 GHz was measured at V_{GS}/V_{DS} = +0.6/1 V, which is enticing for applications demanding high gain with small power consumption.

Benchmarked against the best planar FETs built with VLS NWs, CNTs, or graphene channels, our planar NW array-based HEMT has superior $f_{max}L_G$ as well as the highest I_{ON}/I_{OFF} (Figure 5). It should be noted that the high $f_{max}L_G$ was obtained despite having large parasitic capacitance. Analyzing

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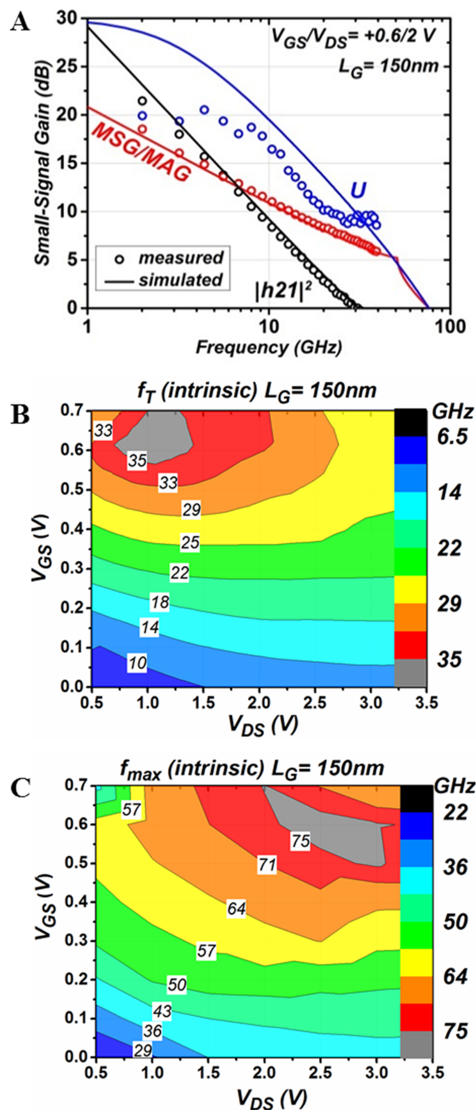

Figure 4. RF performance of planar NW array-based HEMTs. (A) Measured and simulated small signal gain versus frequency for L_G = 150 nm and V_{DS} = 2 V. Contour plots of f_T (B) and f_{max} (C) as a function of gate and drain voltage for L_G = 150 nm.

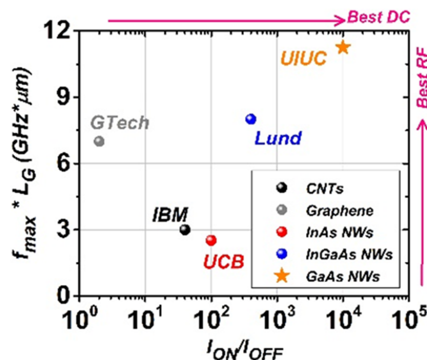

Figure 5. DC and RF performance benchmark of the best planar FETs built with VLS NWs, CNTs, or graphene channels evaluated by I_{ON}/I_{OFF} and $f_{max}L_G$. The planar NW array-based HEMT ranks among the best reported in literature.

with an equivalent circuit small-signal model (see Supporting Information), we found the intrinsic gate-to-channel capacitance accounts for only 17% of the total gate capacitance. Eliminating the parasitic capacitance, we extracted a high intrinsic velocity of ~1.49 × 10^7 cm/s (at V_{DS}= 1 V), which yields speed exceeding 0.3 THz (see Supporting Information). The large parasitic capacitance is attributed to the low NW density (~1.5 NWs/μm), which can be largely reduced by enabling the unidirectional planar NW growth and using a tight NW pitch.[46] In our previous study using randomly dispersed Au colloids as the growth seeds, unidirectional planar GaAs NWs[42] and planar NWs with sub-50 nm sizes and sub-20 nm pitches have all been demonstrated.[37] Thus, given finer patterning, high-density unidirectional planar NW arrays should be a viable option in the future to reduce parasitic capacitance. By using smaller planar NWs in the channel and thinner barrier layer with sufficient delta doping, the dimensions of the devices, such as L_G and source-to-drain separation, can be down-scaled while maintaining good electrostatics. With future iterations such as high-k dielectric gate integration and growth enablement of planar In(Ga)As NW arrays,[47] our bottom-up planar NW technology has a clear roadmap to meet both the digital and RF requirements for future SOC applications.

Conclusions and Remarks. Through the demonstration of wafer-scale planar GaAs NW arrays with ~100% yield and precise NW site and size control, we have provided evidence that our planar NW technology is a viable option for large-scale electronic device applications. For the first time, planar NW technology was used to demonstrate array-based HEMTs with large number of identical GaAs NWs self-assembled in-plane with the substrate and sufficiently long for double-channel RF device fabrication. Benchmarking against the existing planar FETs with VLS NWs, CNTs, or graphene channels, our planar NW array-based HEMTs show the best DC (I_{ON}/I_{OFF}) and RF ($f_{max}L_G$) performances, despite the unoptimized device layout. The excellent device metrics are not only obtainable from a hero device but from the majority of the 115 devices on a 1.5 × 1.5 cm^2 device chip. Our planar NW technology overcomes the ubiquitous challenge of aligning III–V NWs or CNTs with deterministic positions in-plane with the substrates, and is well positioned for post-Si large-scale nanoelectronics.

Methods. *Growth of Planar NW Array-Based HEMTs.* Prior to the MOCVD growth, alignment markers were etched into the SI (100) GaAs substrates using a PlasmaTherm 770 inductively coupled plasma (ICP) etching system with an optically defined pattern and AZ-5214 photoresist as the etch mask. The ICP etch settings were $BCl_3/Cl_2/Ar$ 10/5/5 sccm at 150 W. Then, Au seeds with 100 nm diameter, 300 nm center-to-center separation and 30 nm height were formed by EBL, Au deposition (30 nm) and lift-off processes. A stringent cleaning process of repeating 10 min soaks in PG remover solvent was carried out before loading the sample in an Aixtron 200/4 MOCVD reactor. Trimethyl-gallium (TMGa), trimethyl-aluminum (TMAl), AsH_3, and Si_2H_6 were used as the precursors for Ga, Al, As, and Si. Oxide desorption was carried out at 625 °C for 10 min with AsH_3 overpressure. The reactor pressure and temperature were then brought to 950 mbar and 450 °C for VLS NW growth. Constant flows of 10-sccm TMGa (1.16 × 10^{-4} mol/min) and 10 sccm AsH_3 (4.46 × 10^{-4} mol/min) were used in the 200 s VLS GaAs NW growth. In the NW growth, reactor temperature was initially kept at 450 °C for 20 s, then dropped linearly to 430 °C in 60 s and maintained at 430 °C for another 120 s. With such two-temperature-step VLS growth method, planar GaAs NW arrays with ~100% yield and high crystal quality were achieved. After the VLS NW growth,

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the reactor pressure was adjusted to 100 mbar; and reactor temperature was elevated for epitaxial thin film growth. A 3 nm undoped $Al_{0.33}Ga_{0.67}As$ layer was grown at 500 °C to stabilize the surface atoms of GaAs NWs and preserve NWs' original 3D morphology from the following high temperature growth. The 50 nm Si-doped (3×10^{18} cm^{-3}) $Al_{0.33}Ga_{0.67}As$ barrier layer and 50 nm n$^+$ (5×10^{18} cm^{-3}) GaAs ohmic contact layer were grown at 680 °C for high doping efficiency.

Fabrication of Planar NW Array-Based HEMTs. Ohmic contacts were deposited using an EBL pattern and metal evaporation and lift-off of Ni/Ge/Au/Ni/Au. The sample was alloyed at 400 °C for 20 s in hydrogen in a lab-built annealing system. Next, an optically defined mesa wet-etch step using $H_2SO_4/H_2O_2/H_2O$ (1:8:80) for 20 s was achieved. The pad metal was deposited using optical lithography, metal evaporation, and lift-off of Ti/Au. The next step was EBL of the T-gate which consisted of exposing and developing a trilayer PMMA/MMA/PMMA resist stack. Finally, gate recess etching was done in citric acid/H_2O_2 (4:1) for 7 s and followed by metal evaporation and lift-off of Ti/Pt/Au.

DC/RF Characterization of Planar NW Array-Based HEMTs. RF measurements were performed using reticle step automation on a Cascade Microtech probe station with Agilent Technologies E8364B network analyzer with bias tees connecting to a semiconductor parametric analyzer. Off-chip short-open-load-thru calibration was used to de-embed up to the probe tips while on-wafer open and short structures were used to de-embed the device pad capacitance. The RF settings were −27 dBm input power and the frequency range was 0.01−40 GHz.

TEM Characterization of Planar NWs. Lamellae for TEM analysis containing single planar NWs were prepared using an FEI Helios NanoLab 600i FIB. HR-TEM characterization was carried out using a JEOL 2010F EF-FEG instrument.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

High-resolution transmission electron microscopy, supplemental static and radio frequency (RF) electrical characterization, and a small-signal RF model. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

[§]X.M. and K.C. contributed equally.

Notes

The authors declare no competing financial interest.

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