This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2016.2577046, IEEE Electron Device Letters

Ultra-high Aspect Ratio InP Junctionless FinFETs by a Novel Wet Etching Method

Yi Song, Parsian K. Mohseni, Seung Hyun Kim, Jae Cheol Shin, Tatsumi Ishihara, Ilesanmi Adesida, *Fellow, IEEE*, and Xiuling Li*, *Senior Member, IEEE*

***Abstract*—Junctionless FinFETs with an array of ultra-high aspect ratio (HAR) fins, enabled by inverse metal-assisted chemical etching, are developed to achieve high on-current per fin. The novel device fabrication process eliminates dry etching-induced plasma damage, high energy ion implantation damage, and high temperature annealing thermal budget, ensuring interface quality between the high-k gate dielectric and the HAR fin channel. Indium phosphide (InP) junctionless FinFETs, of record HAR (as high as 50:1) fins, are demonstrated for the first time with excellent subthreshold slope (63 mV/dec) and on/off ratio (3×10^5).**

***Index Terms*—FinFET, high aspect ratio, metal-assisted chemical etching, junctionless, interface states, nanofabrication.**

I. Introduction

FinFET, which uses a double or tri-gate surrounding the fin channel to enhance gate electrostatic control over the channel, has become the mainstream technology for state-of-art transistor scaling [1]. Significant challenges remain in meeting the aggressively demanding dimensional and performance requirements for future generations beyond the 14 or 10 nm node using FinFETs [2]. Dry etching-induced surface damage and its non-vertical profile are some of the most serious problems for multigate FinFETs, especially for post-Si CMOS technologies using high mobility III-V compound semiconductors [3, 4]. In addition, in aggressively scaled CMOS circuits, the effect of interconnections is getting more and more pronounced since the transistor is getting smaller and more crowded such that RC delay associated with the increased number of interconnection layers increases [5]. Therefore, an even stronger demand for high drive current per unit area is required in order to compensate for the interconnection delay.

One can use multiple planar channels stacked in the vertical direction [6, 7] or densely packed vertical nanowire channels [8] to increase current density per chip surface area. Both of these device geometries obviously require complicated growth or process flows and faces poor uniformity issues. Ultra-high aspect ratio (HAR) FinFET is a more straight forward way to boost current density for a given surface area. However, it is extremely challenging to fabricate conventional inversion-mode FinFETs of ultra-HARs. This is because deep source and drain (S/D) doping profiles in ultra-HAR FinFETs would require deep implantation that is normally achieved with high energy ions and high temperature annealing. These steps can potentially create severe crystal damage and high thermal budget-related compatibility issues. In addition, doping uniformity would be difficult to control over the entire depth. Also, scaling the channel length while preventing S/D punch-through throughout the depth direction is nearly impossible due to the deep S/D junction. To avoid these difficulties, the junctionless transistor structure [9-11] which does not require lateral p-n junctions, should be used for ultra-HAR FinFETs.

In this paper, we demonstrate extremely HAR (as high as 50:1) junctionless InP FinFETs with near-ideal subthreshold slope (63 mV/dec) and on/off current ratio of 3×10^5, enabled by a novel wet etching method, inverse metal-assisted chemical etching (i-MacEtch) for the first time. This demonstration confirms that, beyond channel length scaling, ultra-HAR FinFETs are a feasible route to deliver high current while maintaining excellent gate electrostatic control.

II. Device Fabrication

Fig. 1 presents a schematic view of the process flow for fabricating a HAR InP FinFET. A 600 nm thick InP epitaxial layer (n type, Si-doped, 8×10^{17} cm^{-3}) was first grown by MOCVD on a semi-insulating InP substrate (Fig. 1(a)). The device area was defined by e-beam lithography patterning into parallel stripe openings, followed by a 30-nm Au layer deposition by e-beam evaporation and subsequent lift-off process to form the Au strips on top of the substrate (Fig. 1(b)). This was followed by the i-MacEtch [12, 13] process to form the InP fins in Fig. 1(c), where Au served as the catalyst to initiate the local electrochemical etching of InP in the solution of H_2SO_4 and H_2O_2. In contrast to conventional forward MacEtch [14, 15], Au was employed here as a catalytic mask to induce material dissolution starting from the off-metal areas, i.e. inverse MacEtch (i-MacEtch). In this manner, time-controlled etching allowed for the formation of localized nanofin array structures, predefined by the location of Au catalyst patterns. The S/D region was intentionally made wider than the channel region to reduce parasitic resistance by simply modifying the metal pattern layout, which is an inherent merit of i-MacEtch. After the doped epitaxial layer (600 nm) was reached, an intentional over etching (100 nm) into the insulating substrate was done to make sure that the fin channel was fully isolated from the substrate. The etching process was performed at room temperature effectively prohibited gold from diffusion into InP. After etching, Au was removed (Fig.

This work was supported in part by NSF CMMI #14-62946 and the International Institute for Carbon-Neutral Energy Research (I2CNER).

Y. Song, P. K. Mohseni, S. K. Kim, I. Adesida and X. Li are with the Department of Electrical and Computer Engineering, and Micro and Nanotechnology laboratory, University of Illinois at Urbana-Champaign, Urbana, IL, 61801, USA (email: xiuling@illinois.edu). P. K. Mohseni is now with Rochester Institute of Technology, Rochester, NY, 14623, USA. J. C. Shin is with Yeungnam University, Gyeongsan-si, Gyeongsangbuk-do, Republic of Korea. I. Ishihara is with I2CNER, Kyushu University, 744 Moto-oka, Nishi-ku, Fukuoka 819-0395, Japan. X. Li is also affiliated with I2CNER.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier.

0741-3106 (c) 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2016.2577046, IEEE Electron Device Letters

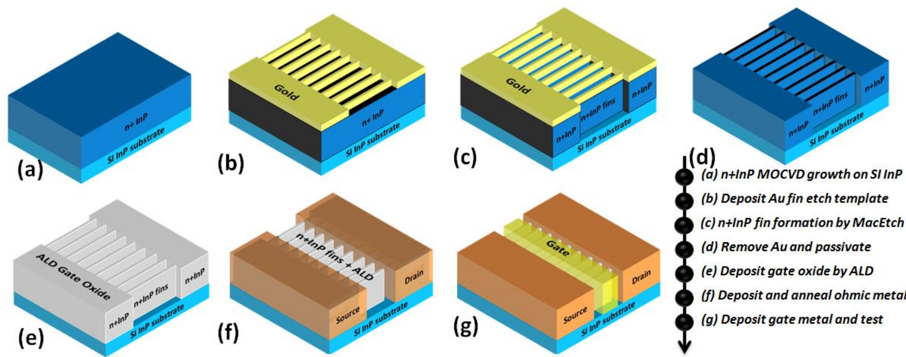

Fig. 1: Schematic diagram and the corresponding description of the process flow (a)-(g) for the fabrication of an InP junctionless-MOSFET by i-MacEtch.

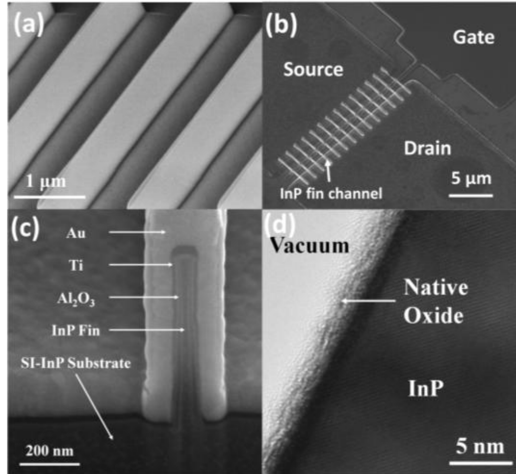

Fig. 2 Structure characterization: (a) 45° tilted-view SEM image of an array of InP fins. (b) Titled top-view SEM image of a fully-fabricated device. (c) 52° tilted-view SEM image showing the cross-section of a 14 nm wide 700 nm tall InP fin with Al_2O_3 high-k and Ti/Au metal gate. (d) HR-TEM image showing the smooth sidewall after i-MacEtch.

1(d)) by standard Au etchants (TFA, Transene Co.) without attacking InP.

After dilute HF dipping, surface passivation was first performed in diluted $(NH_4)_2S$ solution, then the samples were immediately loaded into an ALD chamber for Al_2O_3 gate dielectric (~9 nm) deposition, followed by a 30 s RTA at 500 °C (Fig. 1(e)). In order to fully wrap the metal contacts over the high-AR InP fins, tilted sputtering of Ge/Au/Ni/Au for source/drain (S/D) pads (Fig. 1(f)), and Ti/Au (10 nm/100 nm) for the gate metal (Fig. 1(g)) were employed. Before gate deposition, the S/D contacts were annealed by RTA in N_2 at 400 °C for 30 s. Note that metal lift-off above the tall fins is very challenging and for this work, only long channel devices were realized.

Fig. 2 (a) shows the SEM images of an array of InP fins of ~20 nm in width and ~700 nm in height. Fig. 2 (b) shows the corresponding titled top-view of a fully-fabricated InP FinFET structure showing the gate is very well-aligned in the center between source and drain contacts. Fig. 2(c) shows the cross-sectional view of a single fin that is 14 nm wide at its narrowest part and 700 nm tall (AR of 50:1), surrounded by 9 nm high-k Al_2O_3 and 10 nm Ti/100 nm Au gate metal. It can be seen that the gate stack is conformal covering the entire fin, as a result of the isotropic deposition (Al_2O_3) by atomic layer deposition (ALD) and rotated sputtering of the metal layers (Ti/Au). In addition to being free of ion-induced damages, unique to this i-MacEtch technique, the resulting sidewall etching profile is remarkably smooth and independent of the metal pattern edge roughness; this is in contrast to forward MacEtch where the etched sidewall morphology mirrors the metal edge saw-tooth pattern [15]. This is crucial for fin to fin uniformity, reducing performance variations due to interface unevenness and line width fluctuations [16]. A high-resolution transmission electron microscopy (HR-TEM) image of the sidewall of an InP nanostructure fabricated by i-MacEtch is shown in Fig. 2(d), confirms its atomically smooth surface [12].

III. Results and discussion

Fig. 3(a) shows the measured transfer characteristics of an InP FinFET with gate length L_g=560 nm, fin width W_{fin}=20 nm and active fin height H_{fin}=600 nm The drain current, I_D, is plotted as a function of gate-source voltage, V_{gs}, for drain-source voltage, V_{DS} of 0.1, 0.5 and 1.0 V. Fig. 3(b) shows the output characteristics, where I_D is plotted as a function of drain voltage V_{DS}, for the same device. There are 14 fins in each device. I_D was normalized by the total perimeters of all fins, (number of fins) x (perimeter of a single fin). Note that the high negative threshold voltage, V_{th}, observed here probably results from a combination of non-optimized gate metal work function, relatively thick fin body (20 nm), and immobile trapped charges in high-k Al_2O_3. Nonetheless, the device exhibits sharp turn-on and well-behaved pinch-off characteristics with an on/off ratio of ~ 3×10^5.

We first discuss the off-state performance. The total device leakage (~0.01 – 0.1 nA/μm for V_{DS} = 0.1 – 1 V) is at the same level of the substrate leakage (measured on a bare substrate across two contact pads). The off-state current remains constant with V_{gs} under all V_{DS}, implying that the gate-induced barrier lowering is negligible. The measured gate leakage is also quite

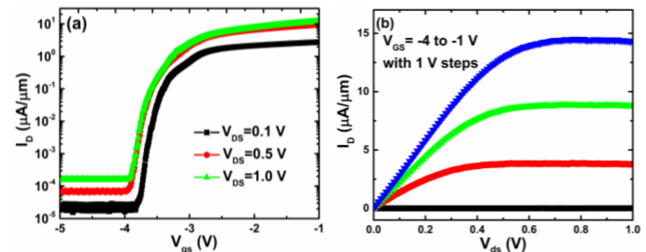

Fig. 3 Measured transfer and output characteristics. (a) I_D-V_{gs} semi-log curves and (b) I_D-V_{ds} curves, of a representative device with L_g=560 nm, W_{fin} = 20 nm and H_{fin}=600 nm, showing abrupt turn on in the subthreshold region. A sharp on/off switch and well-behaved I_{on} saturation is observed.

0741-3106 (c) 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2016.2577046, IEEE Electron Device Letters

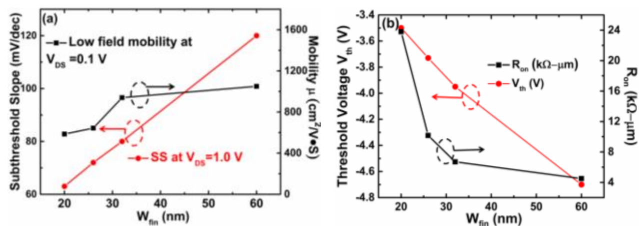

Fig. 4 (a) Measured Subthreshold slope (left axis) and extracted low-field electron mobility μ (right axis) vs. W_{fin}. (b) Threshold voltage V_{th} (left axis) and on-state resistance R_{on} (right axis) vs. W_{fin}. All devices have L_g=560 nm, EOT= 3.9 nm and active fin height H_{fin} = 600 nm.

small (~1pA/μm^2). This confirms that the main device leakage comes from the semi-insulating substrate instead of the fin channels, manifesting the excellent gate electrostatic control of the structure. In addition, no hysteresis was observed in the I_D/V_{gs} curves when sweeping V_{gs} in opposite directions, implying few charge traps at the interface between InP and the high-k dielectric.

Fig. 4(a) shows the minimal sub-threshold slope Ss at V_{DS}=0.1 V (left y-axis) and extracted field effect mobility (right y-axis) as a function of the fin width, W_{fin}. Ss decreases with W_{fin}, as a result of increased gate electrostatic coupling. At W_{fin} of 20 nm, Ss is ~ 63 mV/dec, approaching the ideal value of 60 mV/dec. The estimated D_{it} is low at ~ 2.4×10^{11} cm^{-2}eV^{-1}, since $Ss=(1+q\times A\times D_{it}/C_{ox})\times 60$ mV/dec (A, C_{ox} is the total gate area and gate capacitance respectively). The extracted low field mobility values, estimated from the flat-band I-V equation [9], are in the range of 600-1000 cm^2/V-s for these devices (W_{fin} of 20 - 60 nm), which is higher than the field effect mobility of InP nanowires (200 – 500 cm^2/V-s for 100 nm diameter undoped nanowires [17]) and approaching the measured bulk hall mobility (1780 cm^2/V-s). The excellent off-state performance is direct indication of high interface quality with low mobile charge or trap density between the fin channel surface and the high-k dielectric [18, 19], which can be attributed the atomically smooth and damage-free sidewall surface produced by i-MacEtch.

We now discuss the on-state performance. The drive current I_{on} reaches 7.2 μA per fin or 6 μA/μm when normalized by the gate periphery (Fig. 3(a)), at $V_{DS} = V_{GS}-V_{th} = V_{DD} = 1.0$ V, where $V_{GS} = V_{th}$ was defined when I_D=0.1 μA/μm. The peak transconductance g_m is 14.4 μS per fin or 12 μS/μm by the same normalization method. The I_{on} value per fin achieved is reasonable considering the long channel geometry and un-optimized parasitic resistance especially from the S/D extension region. In fact, it is much higher comparing with that of low aspect ratio junctionless Si FinFETs (0.25 μA per fin at V_{DD}=1.0 V) with gate lengths L_g=1 μm [9] and similar to the stacked Si nanowire channels with L_g=250 nm (20 μA per stack at V_{DD}=1.0 V) [7] and 14 nm node Si FinFET L_g=14 nm technology (33.7 μA per fin at V_{DD}=0.8 V) [2]. The 3-stacked $In_{0.53}Ga_{0.47}As$ nanowire channel with L_c=200 nm and L_g=1 μm, has the highest I_{on} [20] (480 μA per stack at V_{DD}=1.0 V), although the trade-off was a passable Ss and super high off-state leakage.

Due to the extraordinarily HAR of the fin structure, the process challenge to shrink the channel length is significantly increased. For example, a very thick photoresist layer was used in order to cover the entire tall vertical fins, which makes it difficult to scale the lateral dimension. As a result, one major source of the parasitic resistance comes from the large gap (~600 nm) between gate and S/D in our devices due to the non-self-aligned process. $R_{S/D}$ should be around 2/3 of the total on-state resistance R_{on} at flat-band condition since the ungated fin length is almost 2X the channel length for the same fin width (Fig. 2b). Fig. 4(b) plots R_{on}, which was extracted from the linear region of the output curve, and threshold voltage V_{th} as a function of W_{fin}. V_{th} increases as W_{fin} decreases as expected, due to conduction constriction. R_{on} suffers severely from $W_{fin,}$ scaling, as the long ungated S/D extension region also reduces. For the 20 nm W_{fin} device (Fig. 3), R_{on}=23.8 kΩ-μm, and the intrinsic drive current can be projected to reach 18 μA/μm, or 21.6 μA per fin, at V_{DD} = 1.0 V after removing the ungated S/D extension resistance (~ 2/3 of R_{on}). Note that the contact resistance is negligible [21] because it is much smaller than R_{on}.

Therefore, removing the huge parasitic resistance from the ungated S/D extension is a critical issue to address in future work for performance improvement. This can be done by increasing the doping concentration in the S/D extension, developing self-aligned process [22] and advanced 3D patterning to shrink the source to drain distance and achieve short channel devices.

Despite of the un-optimized geometry, it is clear that increasing H_{fin} can indeed boost the absolute value of I_{on}. However, it also proportionally increases the gate intrinsic capacitance C_{gate}, canceling the advantage of I_{on} increase on circuit delay $\tau_{tot}=C_{total}V_{DD}/I_{on}$. The total capacitance in a CMOS logic circuit, $C_{total,}$ is comprised of multiple parts in parallel connection, including interconnect wire lateral capacitance on the same layer and area capacitance between wires on different layers (C_{wire}), parasitic fringing capacitance (C_{fringe}), and C_{gate}. In aggressively scaled CMOS circuits, the effect of interconnect wires becomes more and more prominent, which C_{gate} becomes less significant to C_{total}. Therefore, by increasing H_{fin} (or aspect ratio for the same W_{fin}) while C_{wire} remains constant, I_{on} increases faster than C_{total}, thus the total delay τ_{tot} is reduced. The larger C_{wire} is relative to C_{gate}, the sharper the decrease is in τ_{tot}. Note that C_{wire}/C_{gate} ratio goes up as the technology node scales down, therefore, the benefit of increasing AR in FinFETs should become more pronounced.

IV. CONCLUSION

We have reported the design, fabrication, device performance of ultra-HAR junctionless FinFETs. The device structure was consisted of a uniformly doped extremely-tall fin body as the channel and S/D without p-n junctions. An unconventional wet etching method, i-MacEtch, enabled the fabrication of InP junctionless FinFETs with ultra-high ARs (~50:1). This novel method eliminates the need for dry etching, ion implantation, and minimizes thermal budgets and ion-induced damage, crucial to maintaining high quality surfaces and interfaces. The fabricated devices exhibited high drive current per fin, a near-ideal subthreshold slope, and low leakage current. HAR junctionless FinFETs presented here provide a viable route to achieve high I_{on} transistors and fast delay high speed circuits.

0741-3106 (c) 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2016.2577046, IEEE Electron Device Letters

REFERENCES

[1] C.-H. Jan, U. Bhattacharya, R. Brain, S .- J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J.-Y. Yeh and P. Bai, "A 22nm SoC Platform Technology Featuring 3-D Tri-Gate and High-k/Metal Gate, Optimized for Ultra Low Power, High Performance and High Density SoC Applications," in *IEDM Tech. Dig.,* Dec. 2012 pp. 3.1.1-3.1.4. DOI: 10.1109/IEDM.2012.6478969

[2] C-H. Lin, B. Greene, S. Narasimha, J. Cai, A. Bryant, C. Radens, V. Narayanan, B. Linder, H. Ho, A. Aiyar, E. Alptekin, J-J. An, M. Aquilino, R. Bao, V. Basker, N. Breil, M. Brodsky, W. Chang, L. Clevenger, D. Chidambarrao, C. Christiansen, D. Conklin, C. DeWan, H. Dong, L. Economikos, B. Engel, S. Fang, D. Ferrer, A. Friedman, A. Gabor, F. Guarin, X. Guan, M. Hasanuzzaman, J. Hong, D. Hoyos, B. Jagannathan, S. Jain, S-J. Jeng, J. Johnson, B. Kannan, Y. Ke, B. Khan, B. Kim, S. Koswatta, A. Kumar, T. Kwon, U. Kwon, L. Lanzerotti, H-K Lee, W-H. Lee, A. Levesque, W. Li, Z. Li, W. Liu, S. Mahajan, K. McStay, H. Nayfeh, W. Nicoll, G. Northrop, A. Ogino, C. Pei, S. Polvino, R. Ramachandran, Z. Ren, R. Robison, I. Saraf, V. Sardesai, S. Saudari, D. Schepis, C. Sheraw, S. Siddiqui, L. Song, K. Stein, C. Tran, H. Utomo, R. Vega, G. Wang, H. Wang, W. Wang, X. Wang, D. Wehelle-Gamage, E. Woodard, Y. Xu, Y. Yang, N. Zhan, K. Zhao, C. Zhu, K. Boyd, E. Engbrecht, K. Henson, E. Kaste, S. Krishnan, E. Maciejewski, H. Shang, N. Zamdmer, R. Divakaruni, J. Rice, S. Stiffler and P. Agnello, "High Performance 14nm SOI FinFET CMOS Technology with 0.0174µm2 embedded DRAM and 15 Levels of Cu Metallization," in *IEDM Tech. Dig.,* Dec. 2014 pp. 3.8.1-3.8.34. DOI: 10.1109/IEDM.2014.7046977

[3] T.-W. Kim, D.-H Kim, D.-H. Koh, R. J. W. Hil, R.T.P. Lee, M.H Wong, T. Cunningham, J. A. del Alamo, S. K. Banerjee, S. Oktyabrsky, A. Greene, Y. Ohsawa, Y. Trickett, G Nakamura, Q. Li, K.M. Lau, C. Hobbs, P. D. Kirsch and R. Jammy, "ETB-QW InAs MOSFET with scaled body for improved electrostatics," in *IEDM Tech. Dig.,* Dec. 2012 pp. 32.3.1-32.3.4. DOI: 10.1109/IEDM.2012.6479151

[4] X. Zhao and J. A. del Alamo, "Nanometer-Scale Vertical-Sidewall Reactive Ion Etching of InGaAs for 3-D III-V MOSFETs," *IEEE Electron Device Lett.,* vol. 13, no. 2, pp. 521-523, May 2014. DOI: 10.1109/LED.2014.2313332

[5] D. Hodges, H. Jackson and R. Saleh, Analysis and Design of Digital Integrated Circuits*, 3rd edition. McGraw-Hill Science/Engineering/Math*, 2003.

[6] W. W. Fang, N. Singh, L. K. Bera, H. S. Nguyen, S. C. Rustagi, G. Q. Lo, N. Balasubramanian and D. L. Kwong, "Vertically stacked SiGe nanowire array channel CMOS transistors," *IEEE Electron Device Lett.,* vol. 28, no. 3, pp. 211-213, May 2007. DOI: 10.1109/LED.2007.891268

[7] R. M. Y. Ng., T. Wang, F. Liu, X. Zuo, J. He and M. Chan, "Vertically Stacked Silicon Nanowire Transistors Fabricated by Inductive Plasma Etching and Stress-Limited Oxidation," *IEEE Electron Device Lett.,* vol. 30, no. 5, pp. 520-522, May 2009. DOI: 10.1109/LED.2009.2014975

[8] M. Egard, S. Johansson, A. C. Johansson, K. M. Persson, A. W. Dey, B. M. Borg, C. Thelander, L. E. Wernersson and E. Lind, "Vertical InAs Nanowire Wrap Gate Transistors with f(t) > 7 GHz and f(Max) > 20 GHz," *Nano Lett.* 10, 809–812, (2010). DOI: 10.1021/nl903125m

[9] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nature Nanotech.,* vol. 5, pp. 225-229, Mar. 2010. DOI: 10.1038/nnano.2010.15

[10] S. Migita, Y. Morita, T. Matsukawa, M. Masahara and H. Ota, "Experimental Demonstration of Ultrashort-Channel (3 nm) Junctionless FETs Utilizing Atomically Sharp V-Grooves on SOI," *IEEE Trans.on Nanotech.,* vol. 13, pp. 208-215, Mar. 2014. DOI: 10.1109/TNANO.2013.2296893

[11] Y. Song, C. Zhang, R. Dowdy, K. Chabak, P. K. Mohseni, W. Choi, and X. Li, "III-V Junctionless Gate-All-Around Nanowire MOSFETs for High Linearity Low Power Applications," *IEEE Electron Device Lett.,* vol. 35, no. 10, pp. 324-326, Mar. 2014. DOI: 10.1109/LED.2013.2296556

[12] S. H. Kim, P. K. Mohseni, Y. Song, T. Ishihara and X. Li, "Inverse Metal-Assisted Chemical Etching Produces Smooth High Aspect Ratio InP Nanostructures," *Nano Lett.,* vol. 15, pp. 641-648, Jan. 2015. DOI: 10.1021/nl504136c

[13] X. Li and P. W. Bohn, "Metal-assisted chemical etching in HF/H(2)O(2) produces porous silicon," *Appl. Phys. Lett.,* vol. 77, pp. 2572-2574, Oct. 2000. DOI: 10.1063/1.1319191

[14] K. Balasundaram, J. S. Sadhu, J. C. Shin, B. Azeredo, D. Chanda, M. Malik, K. Hsu, J. A. Rogers, P. Ferreira, S. Sinha and X. Li, "Porosity control in metal-assisted chemical etching of degenerately doped silicon nanowires," *Nanotechnolo.,* vol. 23, 305304, Aug. 2012. DOI: 10.1088/0957-4484/23/30/305304

[15] P. K. Mohseni, S. K. Kim, X. Zhao, K. Balasundaram, J. D. Kim, L. Pan, J. A. Rogers, J. J. Coleman and X. Li, "GaAs pillar array-based light emitting diodes fabricated by metal-assisted chemical etching," *J. Appl. Phys.,* vol. 114, 064909, Aug. 2013. DOI: 10.1063/1.4817424

[16] E. Baravelli, M. Jurczak, N. Speciale, K. D. Meyer and A. Dixit, "Impact of LER and random dopant fluctuations on FinFET matching performance," *IEEE Trans. on Nanotech.,* vol. 7, pp. 291-298, May 2008. DOI: 10.1109/TNANO.2008.917838

[17] J. Wallentin, M. Ek, L. R. Wallenberg, L. Samuelson, and M. T. Borgstrom, "Electron Trapping in InP Nanowire FETs with Stacking Faults," *Nano Lett.* 12, 151–155, (2012). DOI: 10.1021/nl203213d

[18] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature,* vol. 479, pp. 317-323, Nov. 2011. DOI: 10.1038/nature10677

[19] X. Wang, L. Dong, J. Zhang, Y. Liu, P. D. Ye and R. G. Gordon, "Heteroepitaxy of La2O3 and La2-xYxO3 on GaAs (111)A by Atomic Layer Deposition: Achieving Low Interface Trap Density," *Nano Lett.,* vol. 13, pp. 594-599, Feb. 2013. DOI: 10.1021/nl3041349

[20] J. J. Gu, J. J., X. W. Wang, J. Shao, A. T. Neal, M. J. Manfra, R. G. Gordon and P. D. Ye, "III-V Gate-all-around Nanowire MOSFET Process Technology: From 3D to 4D," in *IEDM Tech. Dig.,* Dec. 2012 pp. 23.7.1 -23.7.4. DOI: 10.1109/IEDM.2012.6479091

[21] S. Kim, M. Yokoyama, N. Taoka, R. Iida, S. Lee, R. Nakane, Y. Urabe, N. Miyata, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Takenaka1 and S. Takagi, "Self-aligned metal source/drain InP n-metal-oxide-semiconductor field-effect transistors using Ni-InP metallic alloy," *Appl. Phys. Lett.,* vol. 98, 243501, Jun. 2011. DOI: 10.1063/1.3597228

[22] J. Dunn and G. B. Stringfellow, "Annealed auge based ohmic contacts on InP with Ion milling prior to metallization," *J. Electron. Mater,* vol. 19, no. 2, pp. L1-L3, Feb. 1990. DOI: 10.1007/BF02651748

0741-3106 (c) 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.