Progress Towards Enabling Quantum Engineering

Steve Olson, Chris Hobbs, Hyuncher Chong, Jakub Nalaskowski, Harlan Stamper, John Mucci, Brian Martinick, Karsten Beckmann, Ilyssa Wells, Corbet Johnson, Vidya Kaushik, T. Murray, Steve Novak, Steve Bennett, Martin Rodgers, Chris Borst, Michael Liehr, and Satyavolu Papa Rao (presenting author)

SUNY Polytechnic Institute

Ongoing research at SUNY Polytechnic Institute to enable large scale fabrication of quantum devices with tightly controlled performance characteristics will be presented. Josephson junctions and transmon qubits patterned with 193 nm lithography will be used to illustrate how advanced process tools can control critical dimensions of devices, necessary for building larger ensembles of qubits. Advances in the CMOS industry enable superior surface roughness and interface quality to be achieved across the entire 300mm wafer – some examples will be presented. The integration of photonic circuits (waveguides and on-chip cryogenic IR emitters) with superconducting Josephson junctions to enable large-scale neuromorphic computing structures in the near future will be discussed. Ongoing work on developing materials and processes for UV-transparent photonic circuits at 300mm will be presented – such chips could be useful as part of the interface to trapped ion qubits. The talk will wrap up with a discussion of the synergies in technology development, and functionality integration that can be achieved using an advanced fabrication facility.